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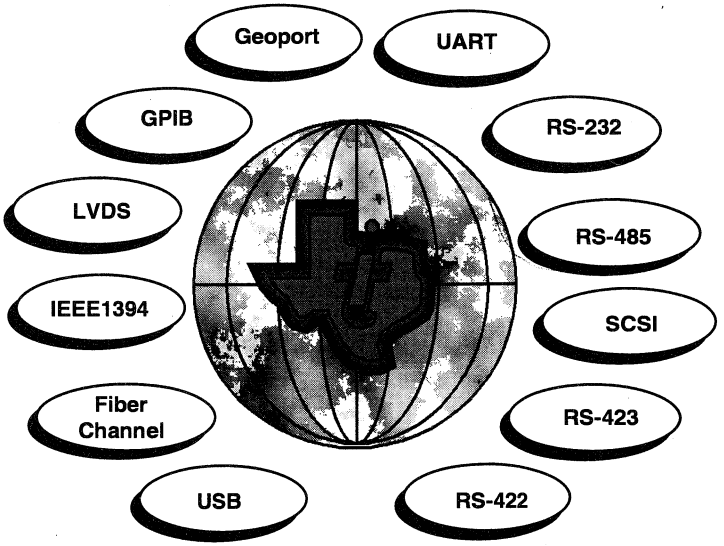
Texas Instruments
Data Transmission Seminar '96



Mixed Signal & Analog Products

TEXAS INSTRUMENTS

1996

DATA TRANSMISSION SEMINAR

contributions by: Eilhard Haseloff
Heinz-Peter Beckemeyer
Jean-Claude Baumer

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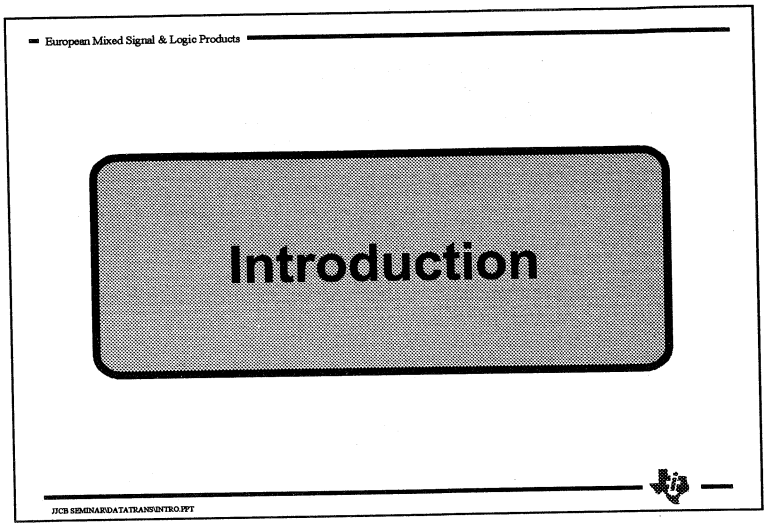
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Introduction
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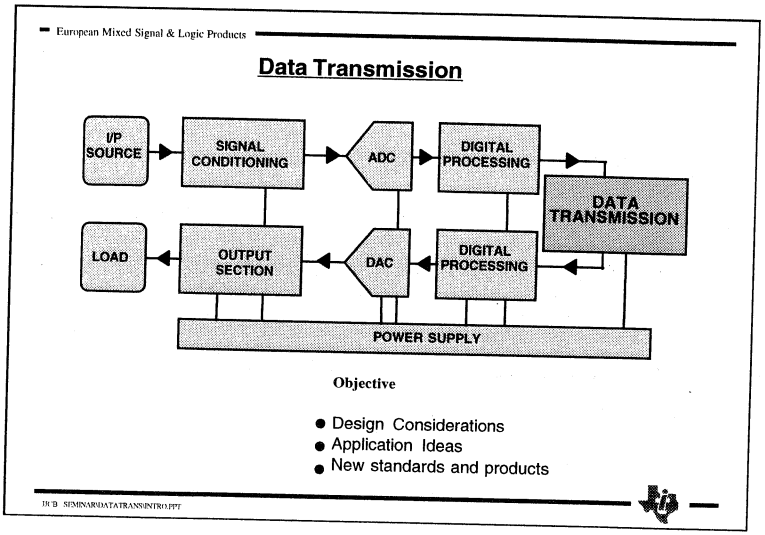


Data Transmission

Data Transmission as part of Texas Instruments' Linear Products portfolio is concerned with the standards involving transmitting data at relatively high speeds down long line lengths, the considerations for which are primarily of an analog more than a digital nature. Likewise the design of data transmission ICs requires experienced analog engineers to implement functions such as slew rate limiting, receiver filtering and common-mode protection.

In this year's seminar we will review single ended transmission standards and differential transmission standards and high speed data transmission protocols. We will explore the circumstances under which to select a given standard and review design considerations when implementing the standard.

The Need for Transmission Standards

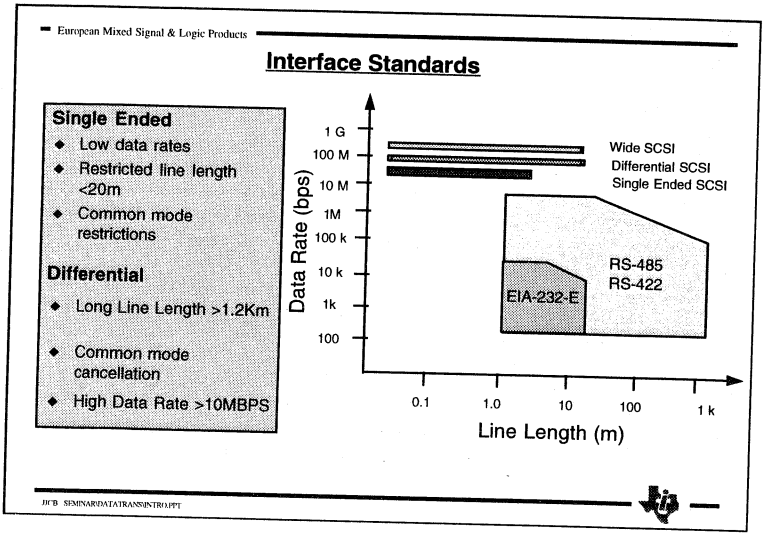
Data transmission standards evolved for two main reasons: From the need to transmit data reliably over long distances, and to provide a standard interface to facilitate communication between equipment from different suppliers. Although TTL/Logic signal levels and products can be used, they generally lack the power handling capabilities, robustness and noise margins required for reliable transmission. Indeed for backplane equipment, TTL is no longer specified for the newer high speed standards, such as Futurebus+ which uses BTL transceivers. In general the standards concerned with transmitting data over long distances incorporate wider voltage swings, increased robustness and higher power outputs than can be delivered using conventional 'Logic' products. Similarly the sub-micron technologies used in the fabrication of today's logic devices cannot provide the power handling and robustness necessary for successful long distance transmission.

Specialised Technologies

This leads to the need for specialist ICs, and technologies, to meet the exacting requirements of these transmission standards. The traditional technological answer has been to utilise the inherent robustness afforded by bipolar technologies, however the additional need for low power consumption and high levels of integration no longer makes this attractive. SC manufacturers are now having to develop their technologies to accommodate these requirements. TI has introduced its proprietary LinBiCMOS* technology combining the robustness of bipolar together with the power consumption and integration afforded by CMOS. Other manufacturers are using pure CMOS and integrating Schottky diodes to the same end. The result is very specialised and reliable products that are able to withstand the harsh environment unique to data transmission products.

Texas Instruments has been a leading supplier of data transmission products for many years, and is continually innovating new fields. Although the following sections are limited to the more common interface standards, TI is actively involved in many new emerging standards and markets, the high speed serial data link evolving from the IEEE1394 committee and multiplex wiring systems such as ABUS, CAN and VAN. The reader is advised to contact a TI representative for information on these product areas.

With the considerable expertise in design, product definition and range of technologies Texas Instruments is the ideal choice for supplying your data transmission product requirements.



Types of Transmission

Most commonly transmission of data occurs directly from one logic gate to another. Low power Schottky TTL and HCMOS can operate at clock frequencies of up to 40MHz. Interconnects must be short (a few 100s of millimetres) and special care taken to assure adequate noise margin and minimum line reflections. The higher speeds of Advanced Schottky TTL and ECL gates place even more emphasis on properly terminated, well defined lines.

There are limiting factors to directly driving over longer distances using standard logic devices. The most important of these is the environmental noise level, whether this is directly radiated or by ground shift potentials. The guaranteed noise margin of standard TTL is +/- 0.4V and is insufficient in most applications.

Many specialised data transmission devices have been developed to overcome this problem, they work by increasing the signal level on a line and thereby improving the noise margin. The techniques involved use single ended or differential (balanced) operation with either voltage mode or current mode drive to the line.

Twisted pair and coax lines are used for single ended drive over longer distances but single and multi wire can be used where the data rate is low and line lengths are short. For differential data transmission a twisted pair is normally used.

Single-Ended Transmission

Numerous integrated circuit devices are available for driving single ended data transmission lines. Some are general purpose and others have been designed to meet specific industrial standards.

Advantages and disadvantages of single ended drivers :

Advantages

- Simplicity : minimum connections
- Low cost

Disadvantages

- Radiates RFI easily
- Poor noise immunity
- Coax improves noise but is expensive
- Limited line lengths and data rates due to susceptibility to interference signals

Differential (balanced) Transmission

The ability to transmit data from one location to another without errors requires immunity to noise. At high data rates, on long lines or under noisy conditions, differential data transmission has an advantage because it is more immune to noise interference than single-ended transmission.

Voltages induced onto the data lines by ground noise or switching transients appear as common-mode signals at the receiver input. Since the receiver has a differential input it corresponds only to the differential data signal. Differential drivers and receivers can operate safely within specified common-mode voltage ranges. Differential line drivers and receivers are designed for general purpose applications as well as specific standards.

Advantages and disadvantages of differential (balanced) data transmission relative to single ended transmission are :

Advantages

- High common mode noise voltage rejection
- Reduced line radiation - less RFI
- Improved speed capabilities
- Drive longer line lengths

Disadvantages

- Slightly higher costs (sometimes)
- Must be used with twisted pair or other types of balanced transmission lines

Referring to Figure 'Interface Standards' we can see the relationship of each transmission standard when comparing data rate and line length.

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Known Interface Standards

Parameter		EIA-232	RS-423-A	RS-422-A	RS-485
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential
Number of Drivers and Receivers		1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers
Maximum Cable Length (m)		15	1200	1200	1200
Maximum Data Rate (bps)		20 k	100 k	10 M	10 M
Maximum Common-Mode Voltage (V)		+25	+6	6 to −0.25	12 to −7
Driver Output Levels (V)	Unloaded	±5	+3.6	+2	+1.5
	Loaded	±15	+6	±5	+5
Driver Load (Ω)		3 k to 7 k	450 (Min)	100 (Min)	60 (Min)
Driver Slew Rate		30 V/µs (Max.)	External Control	NA	NA
Driver Output Short Circuit Current Limit (mA)		500 to V_{CC}	150 to GND	150 to GND	150 to GND 250 to −7 or 12 V
Driver Output Resistance -	Power on	NA	NA	NA	12 k
High Z state (Ω)	Power off	300	60 k	60 k	12 k
Receiver Input Resistance (Ω)		3 to 7	4	4	12
Receiver Sensitivity		±3 V	±200 mV	±200 mV	±200 mV

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Single Ended Transmission : EIA/TIA-232

EIA-232 or 'Recommended Standard' 232 is defined in the ANSI (American National Standard Institution) specification as "The Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange". The standard employs a single ended serial transmission scheme and outlines the set of rules for exchanging data between computer equipment, originally this being a Computer Terminal (DTE) and a modem (DCE). The standard has evolved over the years with the latest 'E' revision released in July 1991. The standard is now known as EIA/TIA-232-E, with EIA standing for the Electronic Industries Association and TIA for the Telecommunications Industry Association.

As with previous revisions of the standard the maximum data rate is defined as 20 k bits per second (kbps) although there are now a number of software applications that now push this data rate above 200 kbps, well outside the standard. The 'C' revision defined the maximum line length as 15 metres however this failed to comprehend the type of cable used and consequently the load capacitance on the line driver. Both the 'D' and 'E' revisions addressed this by more correctly defining the line length in terms of load capacitance. The maximum load capacitance is specified as 2500 pF that translates using standard cables to between 15 and 20 metres. Line length and data rate are limited as the standard employs single ended communication which is prone to external factors. For longer line lengths and higher data rates a differential balanced line communication link is essential.

Differential Transmission : RS422-A

The balanced transmission line standard EIA RS-422 was developed in 1975 to interface a host computer's data, timing or control lines to its peripherals. The standard was revised (RS-422A) in December 1978 bringing it in line with its present specification.

A RS-422 line allows for only one way communication (simplex) mode. By using a differential twisted pair transmission media (not specified in the standard) and a RS-422 receiver with its minimum 7V common mode voltage capacity it is less susceptible to noise picked up in hostile environments via the long cables allowed by the standard. Each driver can drive up to 10 receivers. The specification in the standard places no restrictions on minimum or maximum operating data rates but rather on the relationship of transition speed to a unit interval. However, data rates up to 10Mbps are supported and a line length up to 1200 metres is given as a guide-line , but not at the maximum data rate.

When operating at low data rates (below 200kps) or at any speed where the ratio of the driver's output rise time to the one way propagation delay time of the cable exceeds ten, the cable will not act as a true transmission line and therefore termination is not absolutely necessary. Under all other conditions, the cable loading can no longer be considered as a lumped parameter but must be considered as a transmission line.

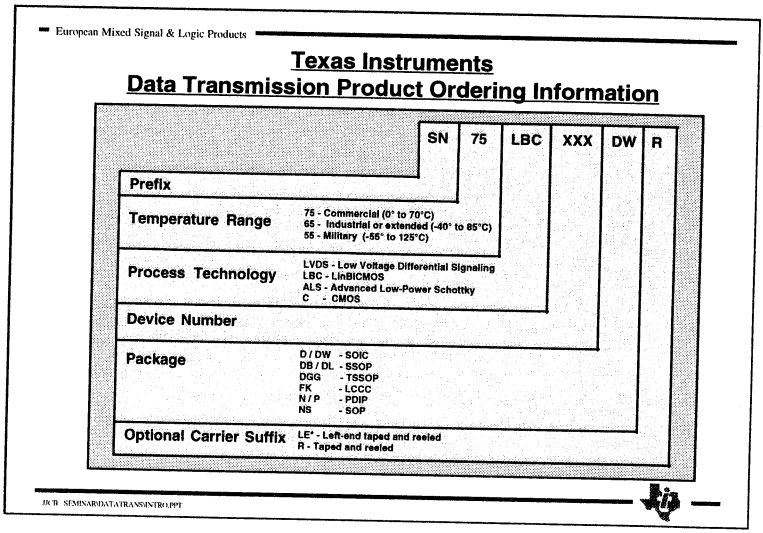
The characteristic impedance of twisted pair cable is a function of frequency and cable type, however typical twisted pair cable impedance's lie in the range 100* to 120*.A termination resistor with an impedance similar to the cable's characteristics impedance should only be connected at the furthest end of the cable.

Differential Transmission : RS-485

RS-485 was primarily an upgrade to the EIA RS-422-A standard utilising the same signal levels but facilitating half duplex multi-point communication. The standard is less complex than the EIA-232 standard as it only specifies the physical layer of the transmission scheme. Hardware such as the connector is left to the user to define. The standard specifies a balanced transmission line whose maximum line length is undefined but is nominally 1.2 km for 24 AWG cable based on 6 dB signal attenuation. The maximum data rate is also undefined but is specified by the relationship of signal rise time to bit time which is influenced both by the line driver and the line length and the line loading. In the majority of applications it is the line length that is the limiting factor on data rate due to signal dispersion. This is discussed in later sections.

Single and Differential Transmission : Small Computer Systems Interface (SCSI)

SCSI is an industry-standard interface, defined by the ANSI, for the interchange of data between computer and computer peripherals. Standard SCSI is a byte wide parallel interface for high speed data transfer over relatively short distances. The SCSI bus is bi-directional and is terminated at both ends of the cable to reduce reflections. For the single ended interface the standard specifies a maximum line length of 6 metres. The maximum data rate is not specified but at present 5 Million Transfers per second (MTps) is achievable using active termination. This can be increased up to 10 MTps using innovative termination as we will discuss later. For longer line length applications, up to 25 metres, the SCSI standard defines the interface using the RS-485 standard as the physical layer. This pushes the data rate to 10 MTps over the full 25 metres which equates to 80 Mbps. A further development of SCSI is 'Wide' SCSI which increases the data bus to 16 bits wide. Using the 10 MTps differential interface this increases the bit rate to 160 Mbps.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Data Transmission Product Ordering Information
SN
75
LBC
XXX
DW
R
Prefix
Temperature Range
75 - Commercial (0° to 70°C)
65 - Industrial or extended (-40° to 85°C)
55 - Military (-55° to 125°C)
Process Technology
LVDS - Low Voltage Differential Signaling
LBC - LinBICMOS
ALS - Advanced Low-Power Schottky
C - CMOS
Device Number
Package
D / DW - SOIC
DB / DL - SSOP
DGG - TSSOP
FK - LCCC
N / P - PDIP
NS - SOP
Optional Carrier Suffix
LE* - Left-end taped and reeled
R - Taped and reeled
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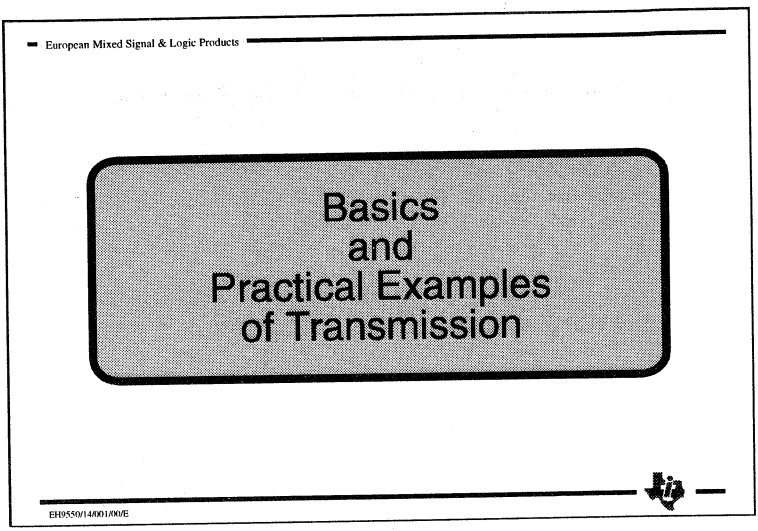
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Basics
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Practical Examples
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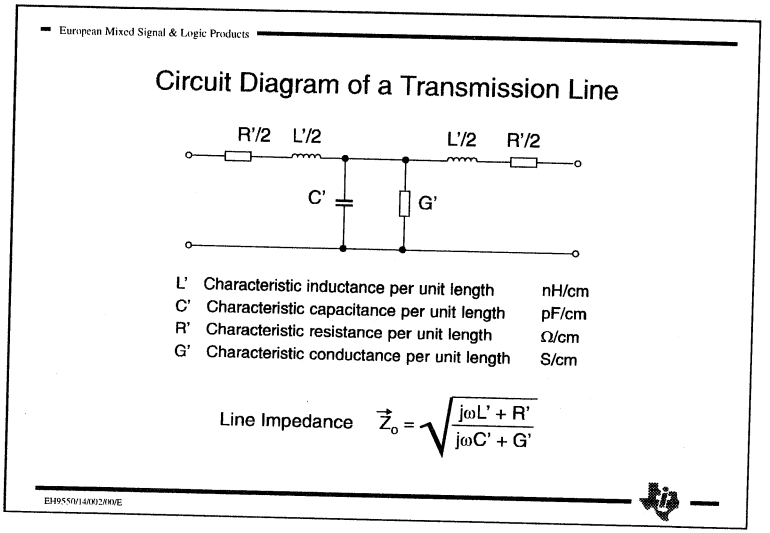

Basics and Practical examples of Data Transmission

Circuit diagram of a Transmission Line (14002)

The equivalent circuit of a transmission line consists of an inductance L' - representing the inductance of the transmission line -, a resistor R' - representing the ohmic resistance of the line, a capacitance C' - representing the capacitance of the line - and the conductance G' representing the losses in the capacitance of the line. All these values are length dependent and are therefore specified in unit/length, e.g.: nH/cm, pF/cm, Ω/cm, and S/cm. By setting up a set of differential equations, one can calculate the impedance of a transmission line:

$$Z_o = \sqrt{\frac{j\omega L' + R'}{j\omega C' + G'}}$$

In practice this equation is difficult to handle. First the line impedance results in a complex number which makes the required calculations time consuming. Second the line impedance is frequency dependent. This fact becomes uncomfortable in digital circuit, where one has to consider many frequencies simultaneously.

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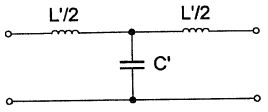
Loss-free Transmission Lines

At high frequencies the transmission line losses (R', G') can be neglected compared with the impedance of the inductance ad the conductance of the capacitance.



With R' << jωL' and G' << jωC':

Line impedance $Z_o = \sqrt{\frac{L'}{C'}}$ (real number!)

Propagation time $t_p = \sqrt{L' \times C'}$

EH9550/14/003/00/E

Loss-Free Transmission Lines

In digital circuits low frequencies are not generally of concern. At higher frequencies (above some 10 kHz) the impedance of the inductance jωL' becomes large compared to the resistance R' of the wire. The admittance jωC' is also much greater than the corresponding conductance G'. Under this assumption R' and G' can be neglected. The impedance of the transmission line can now be calculated by the simple formula

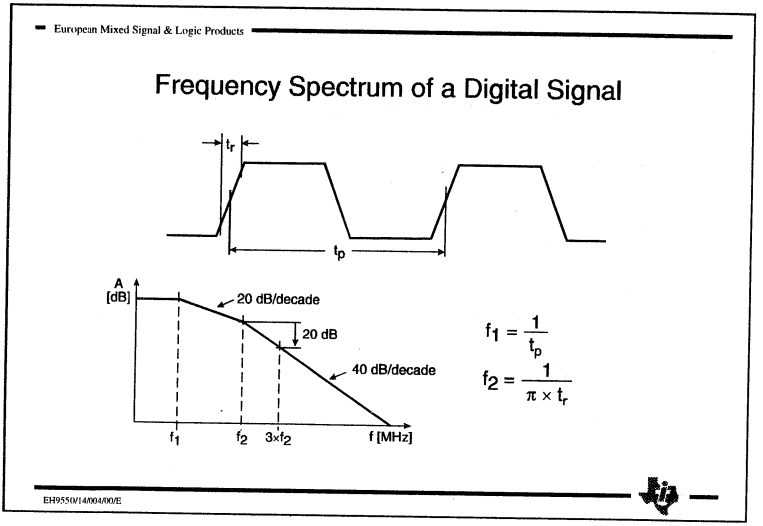
$$Z_o = \sqrt{\frac{L'}{C'}}$$

The impedance is now a real number which can be handled like an ohmic resistor. A further advantage is Z_o is now independent of the frequency.

An important parameter in data transmission circuits is the propagation time t_p of the signal on a transmission line. This time is also determined by the parameters of the line:

$$t_p = \sqrt{L' \cdot C'}$$

On typical cables used in transmission circuits (coaxial cable, twisted pair cable) the propagation time becomes t_p = 5 ns/m. This reflects a propagation speed v = 200 000 km/s (about 60 % of the speed of light)



Frequency Spectrum of a Digital Signal (14004)

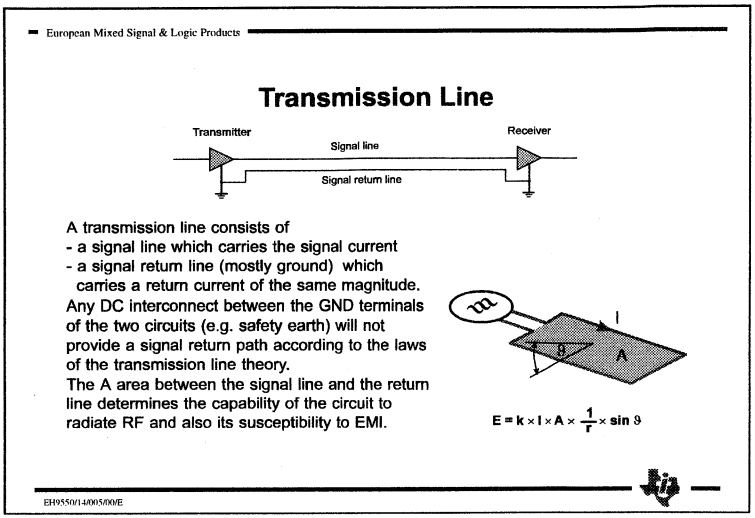
The frequency spectrum of a signal is first determined by the repetition rate of the signal f_1. Above this frequency the amplitude of the overtones drops with 20 dB/decade until a frequency f_2 which is determined by the rise of the signal t_r:

$$f_2 = \frac{1}{\pi \cdot t_r}$$

Assuming the bit rate to be 1 MBit/s, and the rise time of the signal to be t_r = 5 ns, the frequencies are as follows:

f_1 = 500 kHz (50 % of the bit rate) and f_2 = 64 MHz

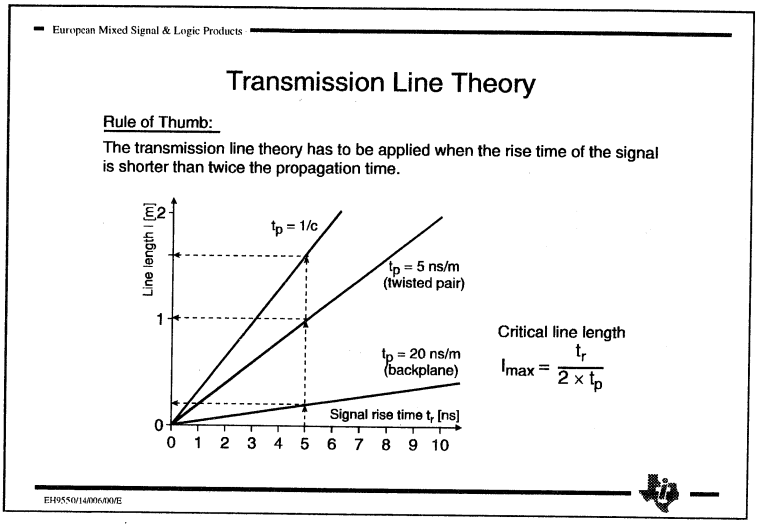
If electromagnetic interference of a transmission system is of concern, the designer can improve the compatibility by either reducing the voltage swing, reducing the data rate, or by selecting interface circuits which provide output signals with a slow rise/fall time.



Transmission Line (14005)

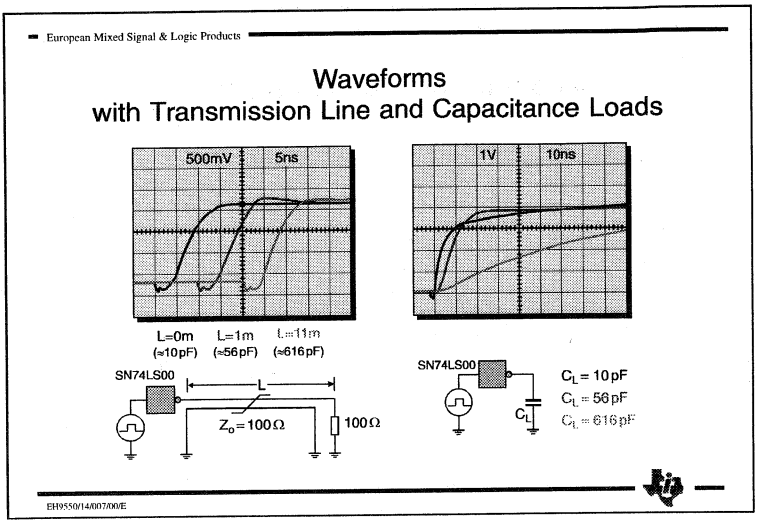
The designer has to keep in mind that a transmission system always has two conductors: the signal line and the signal return line. Both lines have to be designed carefully to ensure the required quality of the interface circuit. Some random signal return path (e.g. via the protective ground wire) is not an adequate signal return line.

Both wires - the signal wire and the signal return wire - act as an antenna which influences the electromagnetic compatibility of the interface circuit. The larger the area between these wires, the larger will be the probability that electromagnetic energy is radiated, which may influence the function of neighbouring equipment. Similarly the area between these wires also determines the electromagnetic susceptibility of the interface circuit.



Transmission line theory (14006)

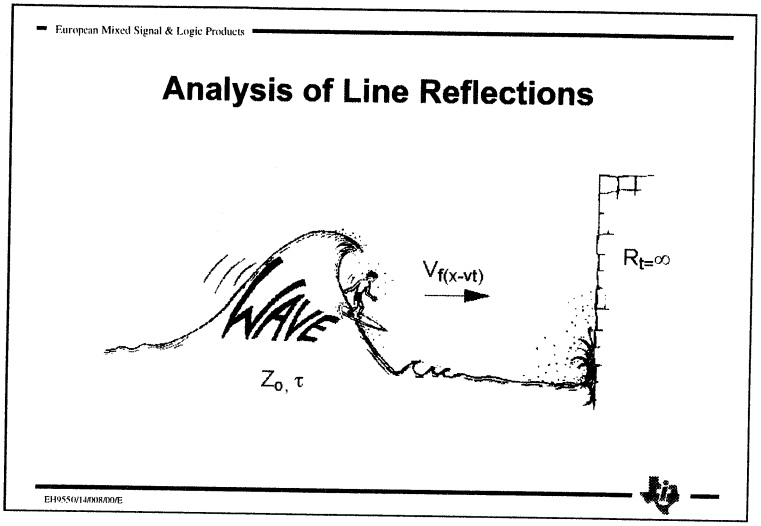
Transmission lines have to be treated as lines in accordance with transmission line theory when twice the signal propagation time becomes longer than the rise time of the signal - i.e.: when the line reflections no longer fall anymore into the rise time interval. For a given rise time t_r = 5 ns and a typical propagation time of the signal t_p = 5 ns/m, the critical line length in l_{max} = 1 m. In applications where the propagation time of the signal is much longer - e.g. bus lines - the critical line length is even shorter.



Wave-forms with Transmission line and Capacitance Loads (14007)

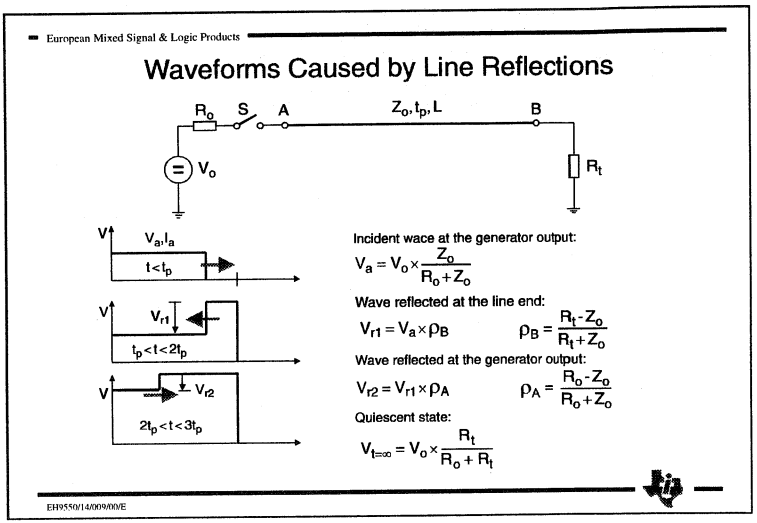
Transmission line theory says that the line impedance is independent of the line length. As a consequence, the loading of the integrated circuit connected to a transmission line must be independent of the line length. The oscillogram above shows the signal wave-forms measured at the output of an integrated circuit (SN74LS00) when terminated transmission lines of various lengths (l = 0 m, l = 1 m, l = 11 m) are connected to the output of the circuit (the line termination is required to avoid line reflections). The three signals measured are displayed with a time offset for visibility. In all cases the rise time of the signal - and that means also the propagation delay time of the integrated circuit - is not influenced by the line length - say: by the capacitance of the line. The designer however has to consider the propagation time of the signal on the transmission line: a line length l = 11 m results in signal propagation time t_p = 55 ns.

A simple capacitive load caused a high input capacitance of the following circuit - e.g. when driving the gate of a MOS power transistor (Miller effect) - in conjunction with the output impedance of the gate ($R_o \approx 150\ \Omega$ for a SN74LS00) generates a low-pass filter, which increases the propagation delay time of the circuit.



Analysis of Line Reflections (14008)

In data transmission systems the designer has to take care of line reflections caused by improperly terminated lines. These line reflections may lead to an additional signal distortion which cause incorrect detection of the value of the signal at the line end (receiver input). This may result in an false operation of the system.



Wave-Forms Caused by Line Reflections (14009)

The circuit above shows a simple circuit arrangement to analyse the wave-form in transmission circuits. At the time the switch at the output of the voltage source (generator) is closed, the effective generator load is the impedance of the transmission line alone. The voltage of the incident wave $V_{a(t=0)}$ can be calculated by using the simple voltage divider formula:

$$V_{a(t=0)} = V_o \frac{Z_o}{Z_o + R_o}$$

When the wave with this amplitude arrives at the line end, the energy not absorbed in the termination resistor - assuming that the line is not terminated correctly ($R_t \neq Z_o$) - will be reflected back to the generator. The amplitude of the reflected wave at that point is calculated:

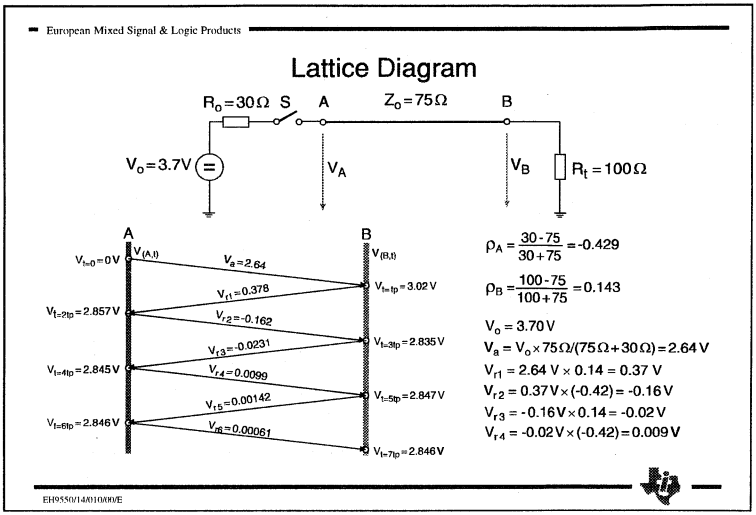
$$V_{r1} = V_a \cdot \rho_B = V_a \frac{R_t - Z_o}{R_t + Z_o}$$

When this reflected wave arrives again at the generator output and the output impedance of the generator is not equal to the line impedance ($R_o \neq Z_o$), again a reflection occurs, where the amplitude of the reflected wave has to be calculated:

$$V_{r2} = V_{r1} \cdot \rho_A = V_a \frac{R_o - Z_o}{R_o + Z_o}$$

This process is continued until the energy of the wave is absorbed by the losses of the circuit (termination resistor R_t at the line end, and output resistor of the generator R_o). The final steady-state condition is calculated by the simple voltage divider:

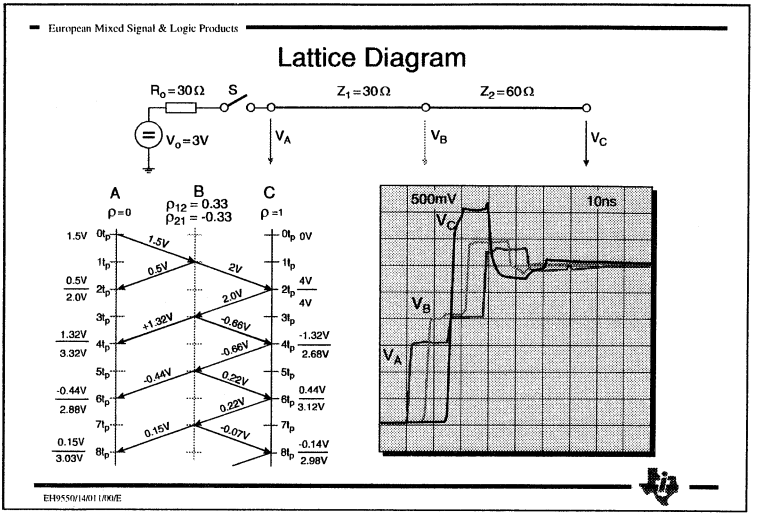
$$V_{t=\infty} = V_o \frac{R_t}{R_o + R_t}$$



Lattice Diagram (14010)

This example shows the analysis of an actual circuit. The generator with an open loop voltage V_o = 3.7 V and an output impedance R_o = 30 Ω represents the simplified equivalent circuit of a SN74F00 in the high state. The line with an impedance Z_o = 75 Ω may be a coax cable or a printed wire on multi-layer printed circuit board. As one can see, the amplitude of the reflected wave drops very fast. In most application the calculation of the various reflected waves can be stopped after the third reflection since the amplitude of the reflected wave is now so small that it can be neglected (in this example V_{r3} = 0.02 V).

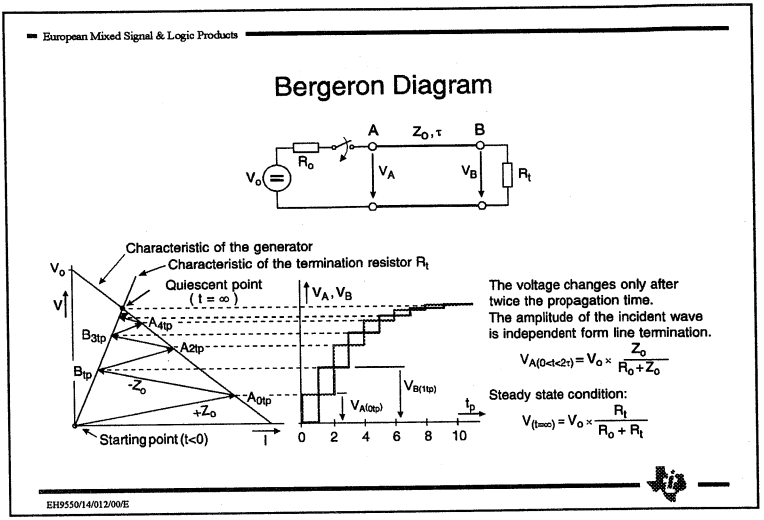
The Lattice Diagram is a useful tool to simplify handling the many numbers to be considered when analysing line reflections. In this simple example the diagram consists of two time scales, each representing the situation at the beginning and at the end of the line. A change of voltage at the generator output is found at every even multiple of the propagation time, at the end of the line at every odd multiple of the propagation time. These points are now connected by lines which represent the forward and backward travelling waves. To each of these lines the corresponding voltage is assigned. The final task left is to add these voltages at the left side of the diagram (beginning of line) of the right side (end of line) to calculate the voltage in the system at a specific time.



Lattice Diagram (14011)

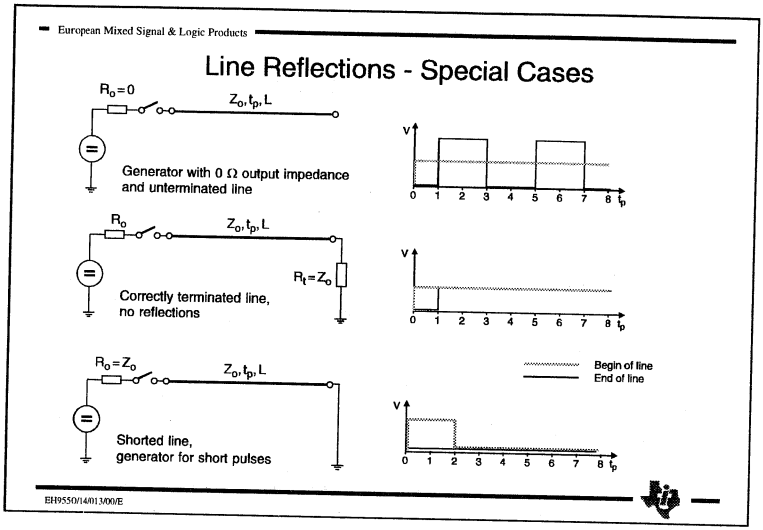
This picture shows a more complex circuit, where two lines of different impedance (Z_1 = 30 Ω, Z_2 = 60 Ω) are connected in series. Situations like this can be found where resistors are not carefully arranged. Another similar situation is found when long stub lines are connected to a trunk cable. This example shows, that the Lattice Diagram can also handle complex waveforms caused by various interfering waves. The transition starts at the generator output with an incident wave amplitude of 3 V, at the line end an overshoot with an amplitude of 4 V is found, while final steady-state voltage will be 3 V.

To simplify the calculation the output impedance of the generator R_o = 30 Ω has been made equal to the line impedance Z_1. Due to this matching the line is terminated correctly (reflection factor ρ = 0) for waves travelling backward into the generator. This avoids reflections at this point of the circuit and eliminates the need also to consider further line reflection caused by this line reflection.



Bergeron Diagram

The Bergeron Diagram is a simple tool to analyse line reflections in circuits which show non-linear characteristics e.g. semiconductor components. For the analysis one has to draw a voltage/current diagram. Into this diagram the output characteristic of the generator R_o (in this example a linear resistor) as well as the characteristic of the termination at the line end R_t has to be drawn. The point of intersection of these two lines provides already the first result: the steady state voltage. The steady-state condition on the line before the switch has been closed ($V_{t=0}$ = 0 V, $I_{t=0}$ = 0 mA) is the starting point for the construction of the wave-form. Through this point (in this example the origin of the diagram) a line with the slope of the line impedance Z_o (tg $\alpha = Z_o$) is drawn. Where this line hits the line which represents the output characteristic of the generator (A_{0tp}), one gets the voltage of the incident wave. By drawing a line with the negative slope (tg a = $-Z_o$) through the point just constructed, the point of intersection (B_{tp}) with the line representing the termination characteristic R_t provides the voltage at the line end, when the wave arrives there the first time. By further drawing lines with alternating slopes (Z_o, $-Z_o$) one finds the voltages in the circuit during the following building-up. Finally the wave-forms at the begin and the end of the line can be constructed by using the voltages found during the previous construction.

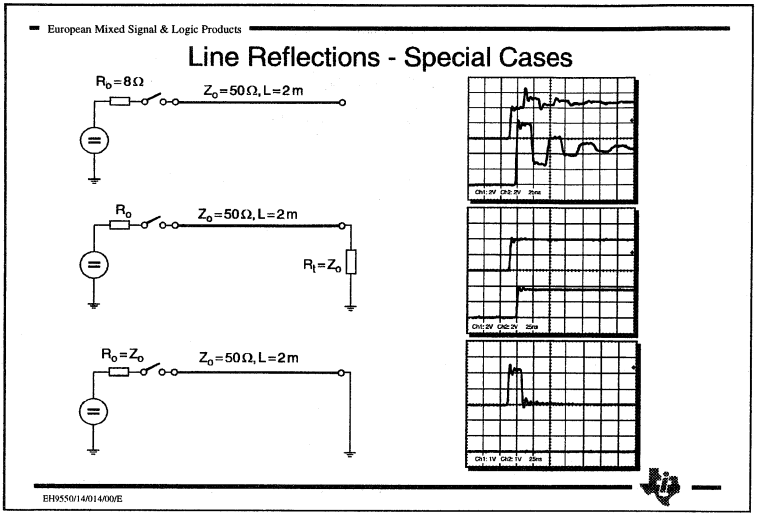


Line Reflections - Special Cases (14013)

This picture shows various extreme situations in transmission circuits. In the first circuit a generator with zero Ohm output impedance (R_o = 0 Ω) drives a loss-free transmission lines, where is an open circuit at the line end ($R_t = \infty$). The open circuit may represents the input impedance of integrated circuits which mostly provide an input impedance of several kilo-ohm - large compared to typical line impedance. The reflection factor $\rho = -1$ at the generator output and $\rho = 1$ at the line end leads to an undamped oscillation at the end of the line. That would cause a receiver to switch many times, but not once only as desired.

The next circuit shows an interface terminated correctly at the line end. Under this condition one finds an undistorted signal (no line reflections)

The last circuit shows and interface shorted at the line end. For simpler understanding the output impedance of the generator has been chosen equal to line impedance ($R_o = Z_o$). When the switch is closed, an incident wave with an amplitude of $0.5 \times V_o$ travels to the line end and is reflected there with the inverted amplitude ($\rho = -1$). When the reflected wave arrives at the generator output again the steady-state is achieved. This circuit is a pulse generator which provides a pulse width equal to twice the propagation time of the wave on the transmission line. Such a circuit can be used advantageously when pulses with a length of a few nanoseconds only have to be generated.

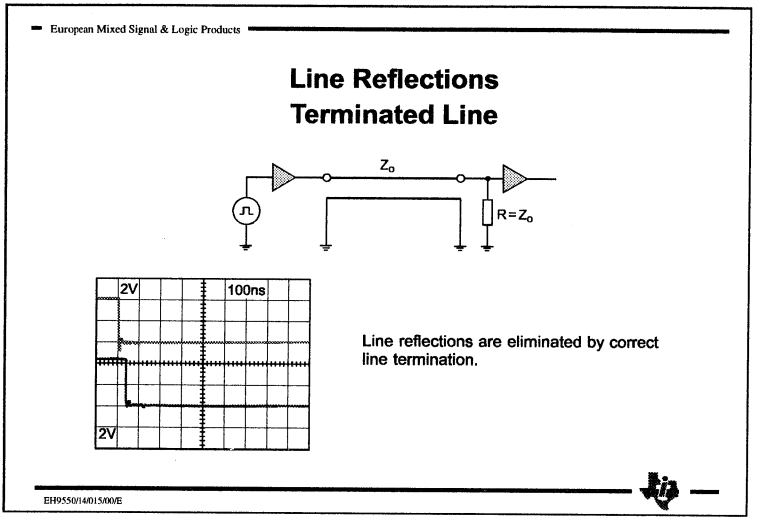


Line Reflections - Special Cases (14014)

The circuits described before have been built up to vary the behaviour. It is not as easy to design an generator with an output impedance of 0 Ω. Therefore an Advanced CMOS circuit has been used as the generator. Its output impedance R_o = 8 Ω leads to a damped oscillation, where the first undershoot at the line may still be capable to reach the threshold voltage of the receiver and to cause a false triggering.

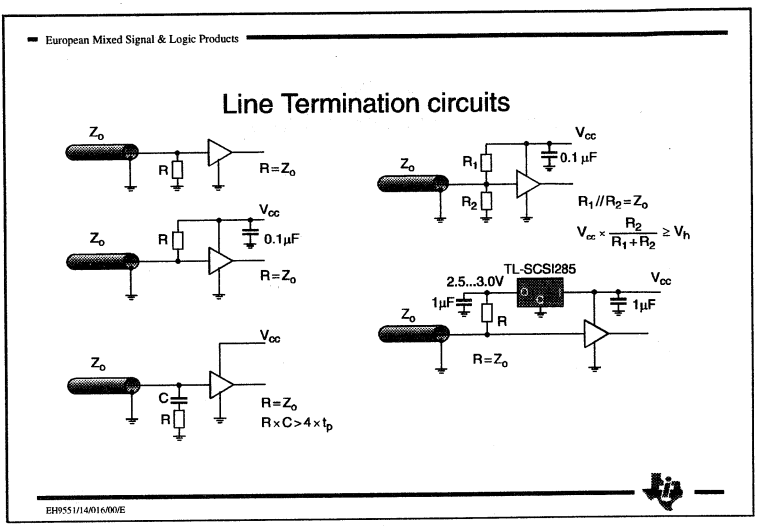
The correctly terminated line shows no signal distortion.

In the interface shorted at the end, a coax cable with a propagation time t_p = 5 ns/m and a length l = 2 m has been used. This circuit generates a pulse with a width $t_d = 2 \times 5$ ns/m $\times$ 2 m = 20 ns.



Line Reflections - Terminated Line (14015)

Transmission lines are terminated at the line end by a resistor between the signal line and the signal return line. If the termination resistor is chosen equal to the line impedance ($R_t = Z_0$) no line reflections are found. In many applications, a mismatch of up to 50 % is acceptable. Under this condition the resulting reflection factor will be $\rho = 0.2$.



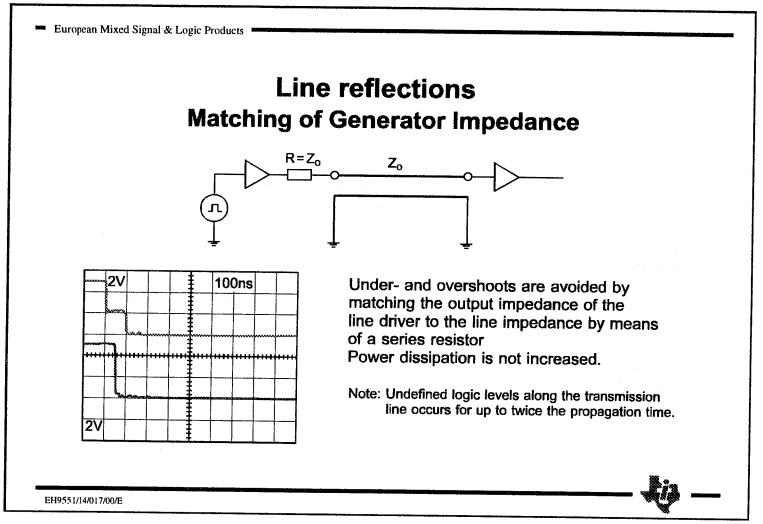
Line Termination Circuits (14016)

Single ended or unbalanced transmission lines are usually terminated by a resistor between the line end and signal ground. If the drive capability of the generator in high state is not sufficient - e.g. circuits with open collector or open drain outputs - the termination resistor can also be placed between the line and the positive supply rail. This rail for low frequencies is shorted to ground via the power supply and for high frequencies via the decoupling capacitor (typical 0.1 µF).

Particularly in CMOS applications, the designer does not like the continuous current in the termination resistor. This current increases the power dissipation. The current can be blocked by placing a capacitor C_b in series to the termination resistor R_t. When the time constant $R_t \times C_b$ is about 4 times the propagation time of the interface circuit, the line is almost sufficiently terminated.

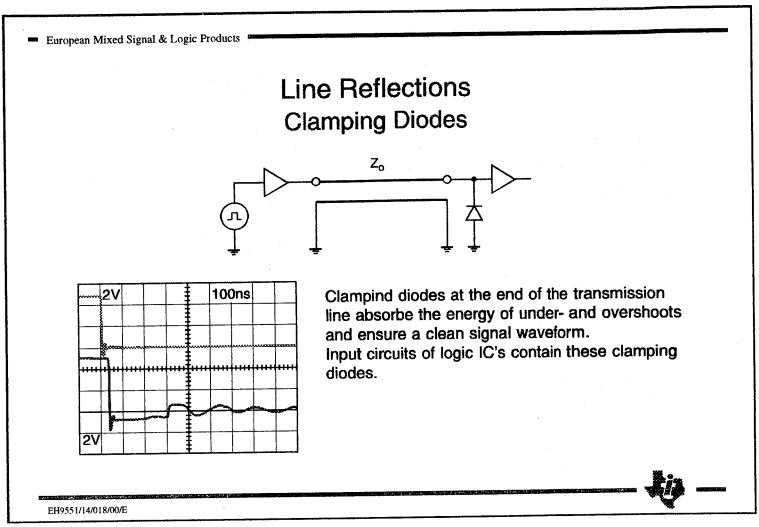
In TTL systems, a resistor divider is often found at the line end (split resistor or Thevenin termination). This circuit is adapted ideally to the drive capability of TTL circuit and performs well in terms of eliminating line reflections. However the disadvantage of this arrangement is the large DC current through the resistor divider.

In advanced interfaces therefore often a circuit is used, which is called Active Termination. Here the termination resistor is placed between the line end and the output of an additional power supply, which provides an output voltage of 2.5 ... 3 V. Since on average 50 % of its active time the line is in the high state, the supply current is reduced by this amount. This termination technique is also used in bus applications, where much of the operating time all bus drivers are in inactive mode (3-state). In this situation the supply current becomes zero. Last but not least, the pull-up resistor avoids the line floating when all bus drivers are in the 3-state.



Line Reflections - Matching of Generator Impedance (14017)

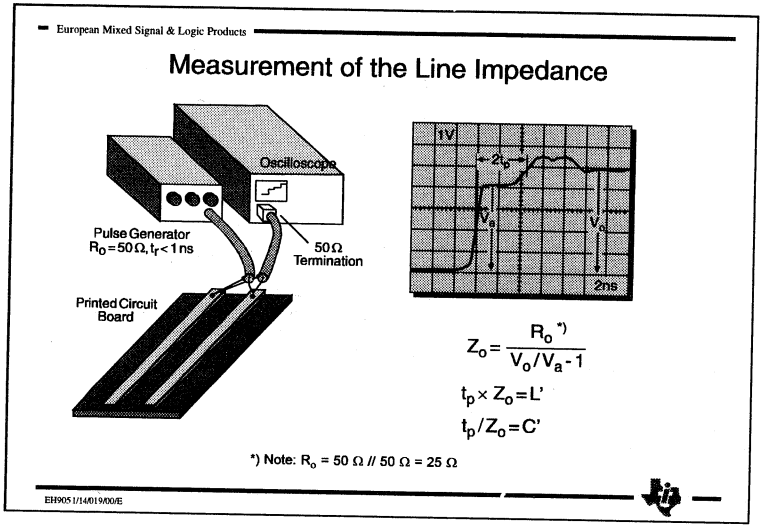
An elegant method to avoid under and overshoots at the line end is to match the output impedance of the driver circuit to the line impedance by placing a resistor in series with the output. A different output impedance of the driver in the low and the high state mostly does not allow correct matching. As long as the output impedance of the circuit in question is chosen to be 60 % to 100 % of the line impedance, a reasonable signal quality can be expected at the line end (receiver input). This technique is applicable in uni- and bi-directional point to point interfaces. In multi-point applications, where several stations are located along the transmission line, this technique is not recommended due to the long settling time of the signal (up to twice the propagation time).



Line Reflections - Clamping Diodes (14018)

An effective method to avoid excessive under- and overshoot at the line end is to limit this by means of clamping diodes. As the picture shows, a negative transition at the begin of the transmission line causes a negative undershoot at the line end which amplitude is limited to the forward voltage of the clamping diode at the line end (≈ 0.7V). The energy stored in the transmission line is not absorbed totally. Therefor one can observe several waves travelling forward and backward on the line. However its amplitude is a few 100 mV only.

Due to the positive influence of these diodes, clamping diodes are integrated into all logic circuits. TTL circuits contain at their inputs clamping diodes to the ground terminal to limit negative undershoots. In a CMOS environment, where due to the higher voltage swing also the positive overshoots are of concern, mostly additional clamping diode between the input and the positive supply rail are incorporated.



Measurement of the Line Impedance (14019)

For a correct design of an interface (selection of the generator, termination of the transmission line), knowledge of the impedance of the transmission line in use is necessary. One way to determine the line impedance is by means of a L/C bridge where one measures the inductance of a transmission line shorted at the end (short circuit impedance ≈ inductive layer L') and capacitance with the line open at the end (open circuit impedance ≈ capacitive layer C'). This method however mostly requires expensive equipment which often is not available.

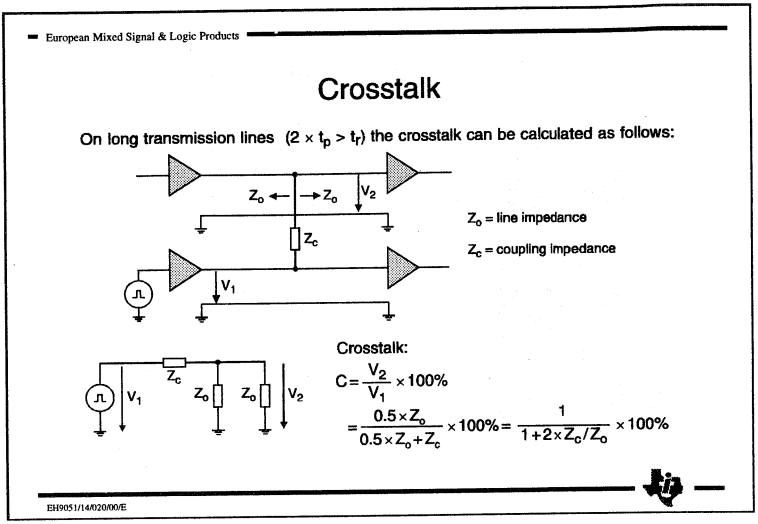
A simpler method is shown on the picture above, where one needs a fast pulse generator and an oscilloscope only. By applying this method one measures the amplitude of the incident wave V_a caused by the voltage divider 'output impedance of the generator / line impedance' (in this example a signal and a ground wire in parallel on a printed circuit board) as well as the steady-state voltage V_o. By using the following equation (the voltage divider formula solved to Z_o) one gets the line impedance Z_o:

$$Z_o = \frac{R_o}{\frac{V_o}{V_a} - 1}$$

where R_o is output impedance of the generator. In this measurement set up the output impedance is made by the two coax cables in parallel, therefore $R_o = 25\ \Omega$.

By measuring the propagation time t_p one can also determine the inductance and the capacitance per unit length:

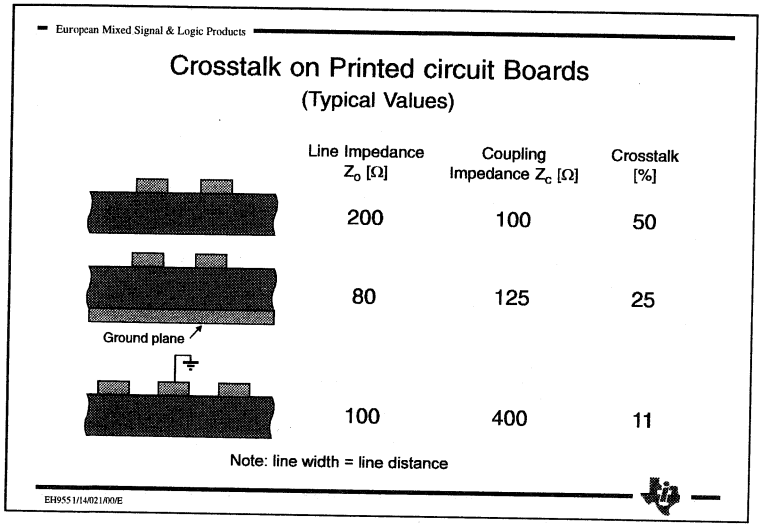
$$L' = t_p \cdot Z_o \qquad C' = \frac{t_p}{Z_o}$$



Crosstalk (14020)

The characteristic of a transmission line can be described by its inductance and capacitance per unit length. When two transmission lines are placed in parallel, one can now define inductance and capacitance per unit length between these two circuits, to give the coupling impedance Z_c. Using this assumption, one can easily describe the crosstalk between interfaces: A signal is transmitted via one line and is coupled via the coupling impedance into the neighbouring line. At the point of coupling the load for the cross-coupled signal is half of the line impedance Z_o (two lines running in opposite direction). The resulting crosstalk can now be calculated by using the following formula:

$$C = \frac{1}{1 + 2\frac{Z_c}{Z_o}}$$



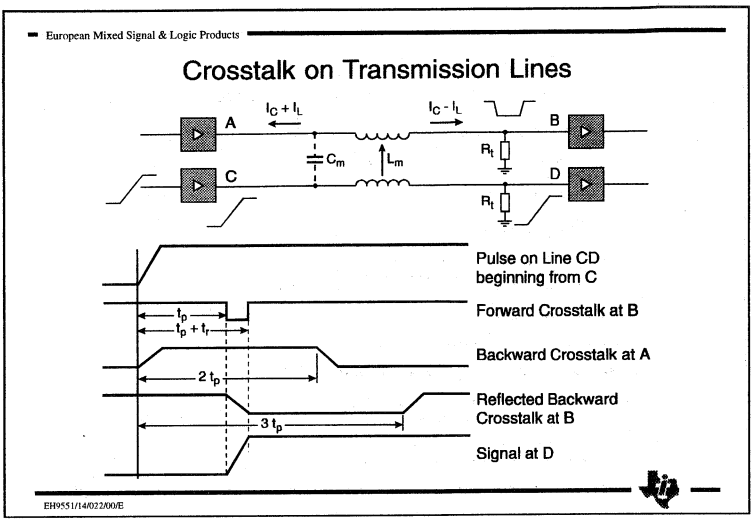
Crosstalk on printed circuit boards (14021)

By applying the formula above, the crosstalk between signal lines on printed circuit boards can be analysed. In the first example two printed wires are running in parallel, with the width of the wires equal to the distance between the wires e.g. 0.5 mm. This arrangement results in a coupling impedance Z_c = 100 Ω. (In the literature dealing with strip lines and microstrips, formulas are shown which allow the calculation of the line impedance based on the physical dimension of the lines). The ground return line is assumed to be far away e.g. 2 cm. This leads to a line impedance of 200 Ω and a crosstalk C = 50 %. Since no logic circuit provides a noise margin of 50 %, such an arrangement is not applicable.

In the second example a ground plane is placed on the opposite side of the printed circuit board. By this the line impedance is lowered to Z_o = 80 Ω, the coupling impedance is increased to Z_c = 125 Ω. The resulting crosstalk is now only 25 %. In digital circuits such value may be acceptable. This example also explains the benefit of a multi layer-board with a ground plane in terms of lowering the noise level in digital circuits.

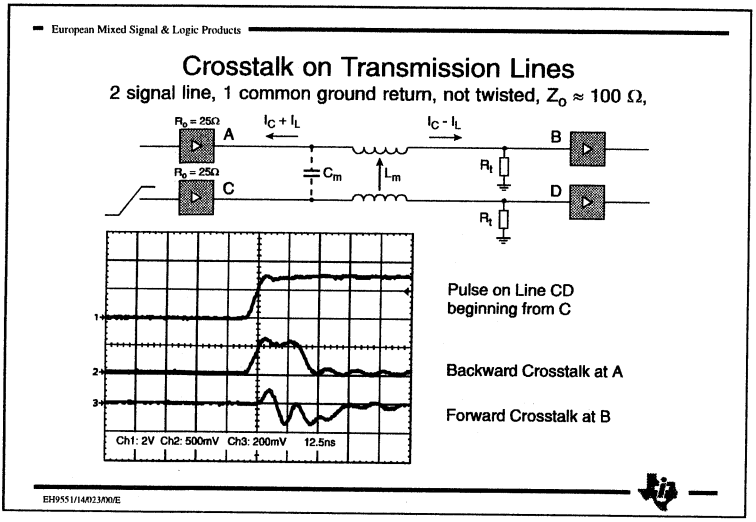
In the third example a shielding wire is placed between the signal lines. (Note: The shielding wire must be connected to ground on both ends.) Again it is assumed, that the line width is equal to line separation. In such an arrangement the line impedance becomes Z_o = 100 Ω and the coupling impedance Z_c = 400 Ω. The resulting crosstalk is lowered to C = 10 %. In digital circuits such a crosstalk is fully acceptable.

This also explains why also twisted pair cables are used for longer lines. One wire of the pair is the signal line, and the other the signal return (ground). Similar behaviour is found, if flat cables are used whith alternate ground and signal lines. Such an arrangement gives a well defined line impedance (Z_o = 80 to 120 Ω) and a low crosstalk. Last but not least, typical crosstalk in a well designed interface will be at least 10 %. This is also valid for the interference between any electrical cable and the interfaces.



Crosstalk on Transmission Lines (14022)

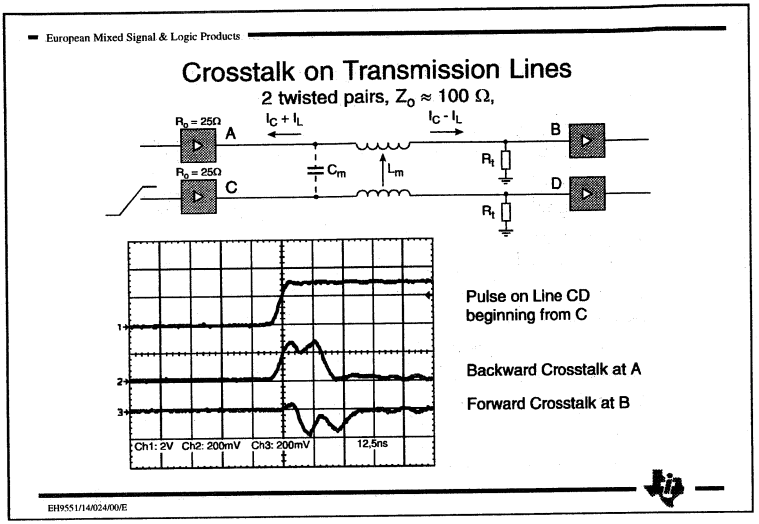
When analysing the crosstalk in more detail, one finds that it induces two currents into the affected line: A current I_C caused by the capacitive crosstalk and a current I_L caused by the inductive crosstalk. When looking from the generator standpoint, the currents travelling down the affected line subtract (I_C - I_L). This results at the end of this line in a relatively small negative noise pulse with a width equal to the rise time of the original signal (forward crosstalk at B in the picture above). In the reverse direction the currents add (I_C + I_L), which leads at the line end near to the generator to a pulse which width is equal to twice the propagation time of signal (Backward crosstalk at A in the picture above). This noise pulse is reflected at the point A and arrives after one propagation time at the far end (Reflected backward crosstalk at B in the picture above).



Crosstalk on Transmission Lines, 3-wire Cable (14023)

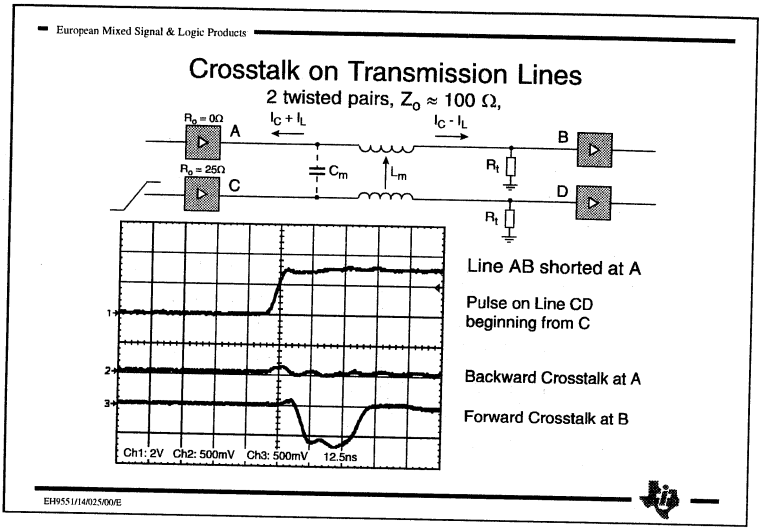
In the following, the behaviour of various circuits arrangements will be analysed. In the first example a transmission line with length 2 m is used which consists of three wires running in parallel (not twisted). The crosscoupled signal at the point B has again a relatively small amplitude which is superimposed on the noise caused by the reflected backward crosstalk at B. Since the generator output impedance at A is smaller than the line impedance, the reflection factor at A becomes negative. This results in a negative amplitude of the forward crosstalk at B.

Note that the three wire circuit used in this application has a similar characteristic to the printed wire circuit with a shielding wire between these two lines (discussed above). The crosstalk is relatively small. In a multi core cable, where only one or a few ground return wires are available, the crosstalk becomes much larger. Under these conditions, reliable operation of the interface can no longer be guaranteed.



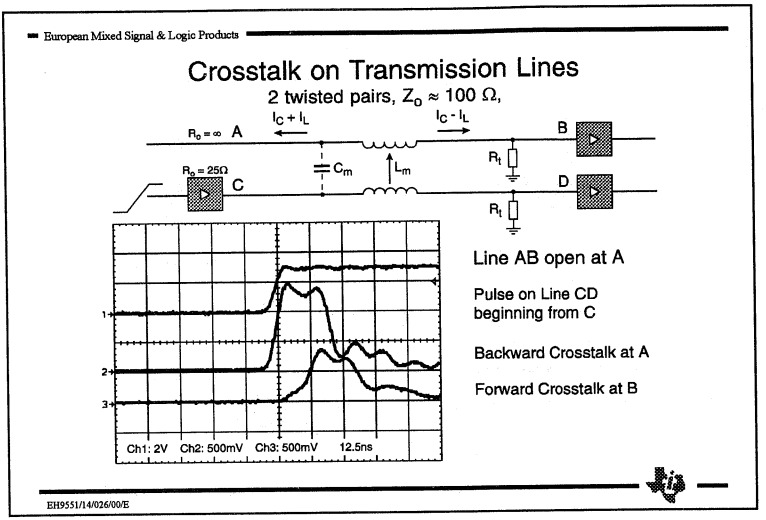
Crosstalk on Transmission Lines, Twisted Pair Cable (14024)

The same circuit arrangement, but using twisted pairs, shows a similar behaviour. The crosstalk at the far end (the receiver at the induced line) again is relatively small. When using twisted pair cables the shielding effect of the many signal return wires keeps the crosstalk at moderately low level even if many pairs are running in parallel in cable.



Crosstalk on Transmission Lines, Near End Impedance = 0 (14025)

It has been shown that the forward crosstalk at the point B is determined to a large degree by the crosstalk reflected at the point B. In the picture above the output impedance of the generator of the affected line is made to zero. Therefore the resulting reflection factor at this point becomes $\rho = -1$. Due to a higher amplitude reflected at this point, the forward crosstalk at the point B also becomes larger. However this example shows an extreme situation. In practise the output impedance of the generator is between 10 and 100 % of the line impedance. This will results in a reflection factor $\rho < -1$, and therefore to a crosscoupled voltage which is significantly smaller.



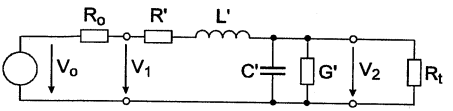
Crosstalk on Transmission Lines, Near End Impedance = ∞

If the output impedance of the generator at the affected line becomes very large (e.g. generator output in 3-state), the reflection factor becomes $\rho = 1$ (positive!). Thus the crosscoupled signal has a large positive amplitude at the point A. This leads also to a positive amplitude of the noise voltage at the pint B. Note the magnitude of the noise voltage at the point B is the same as in the previous example, only the sign of the voltage is different.

Consider also the following situation: Assuming a receiver is located at B where the line is not terminated, the function of the receiver may be affected by the large noise voltage there. (Backward crosstalk at A in the picture above)

European Mixed Signal & Logic Products

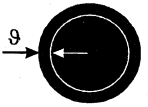
Losses on Transmission Lines



$$V_2 = V_1 \times e^{\frac{-R'}{2 \times Z_o}}$$

Due to the skin effect at frequencies above some hundred kHz only the outer layer of the wire conducts. Thus the losses increase by a factor $\sqrt{f}$.

f (MHz)	ϑ (µm)
1	68
100	6.8
10,000	0.68



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Losses on Transmission Lines

Owing to the ohmic resistance of the wires R', and to a lower degree the conduction G' of the transmission lines, the amplitude of the signal is degraded with increasing line length. The voltage at the line V_2 can be calculated by using the following formula:

$$V_2 = V_1 \cdot e^{\frac{-R' \cdot l}{2 \cdot Z_o} + \frac{-G' \cdot l \cdot Z_o}{2}}$$

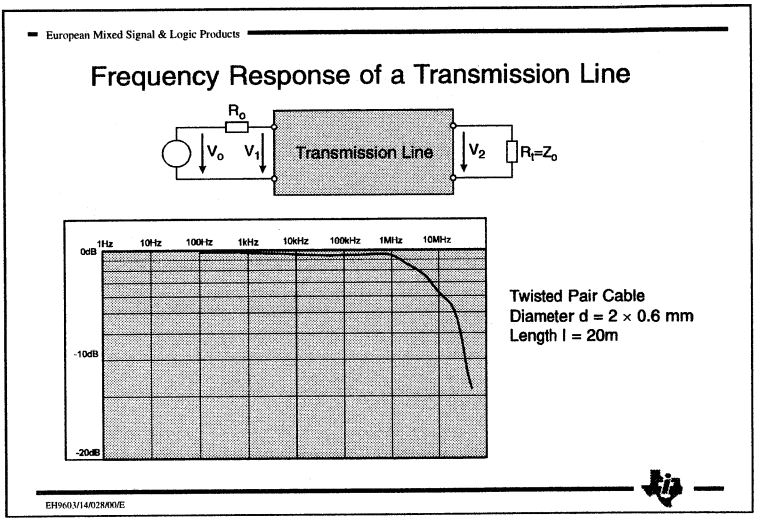
with G' $\rightarrow$ 0 one can simplify the equation:

$$V_2 = V_1 \cdot e^{\frac{-R' \cdot l}{2 \cdot Z_o}}$$

As an example, a transmission line with impedance Z_o = 100 Ω, length l = 1000 m and resistance per unit length R' = 0.1 Ω/m, reduces the voltage at the line end by about 40 %.

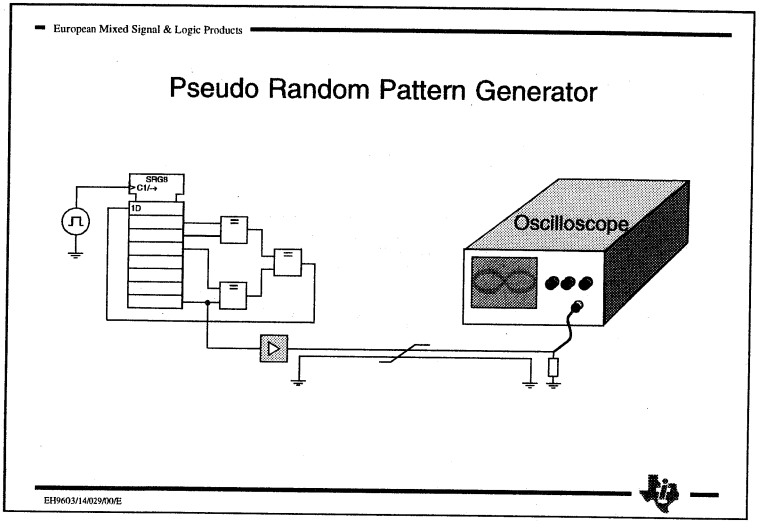
The formula shown above does not consider the so-called Skin Effect. This causes the current to flow only on the surface of the conductor at higher frequencies. This becomes of importance at frequencies > 100 kHz.

Therefore above this frequency the resistance of the wire increases with $\sqrt{f}$.



Frequency response of a Transmission Line (14028)

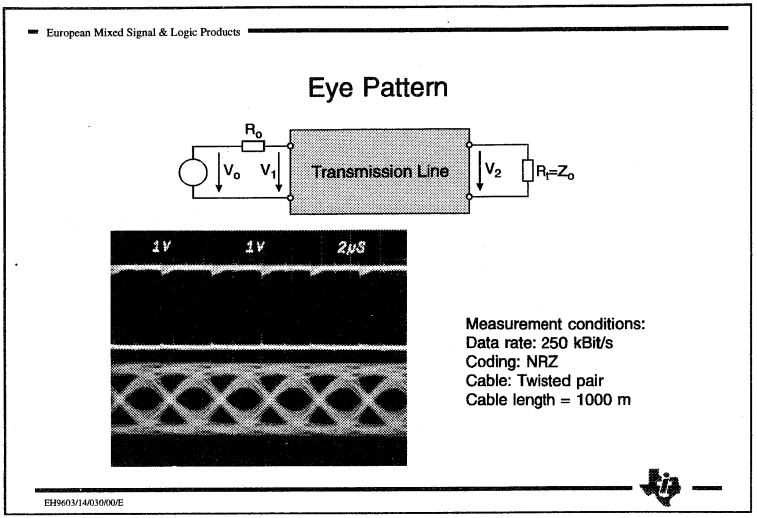
Due to the skin effect, a transmission line has a characteristic similar to a low-pass filter. To analyse the actual behaviour of a transmission line, we measured a twisted pair cable of length l = 20 m and conductor diameter d = 0.6 mm. As can be seen in the picture above, up to a frequency of 1 MHz the losses of the cable remain small. Above 1 MHz however, the attenuation increases considerably.



Pseudo-Ransom Pattern Generator (14029)

In data transmission circuits we have to consider not only discrete frequencies, but a wide frequency band determined by the bit pattern of the data transmitted. Long sequences of ones or zeros represent a low frequency, alternating bit carrying ones and zeros represent a high frequency. Due to the DC content in longer steady states and the filter characteristic of longer lines a DC shift of the average voltage is generated on the transmission line. This DC shift causes the effective amplitude of the signal and the required threshold voltages of the receiver to fluctuate.

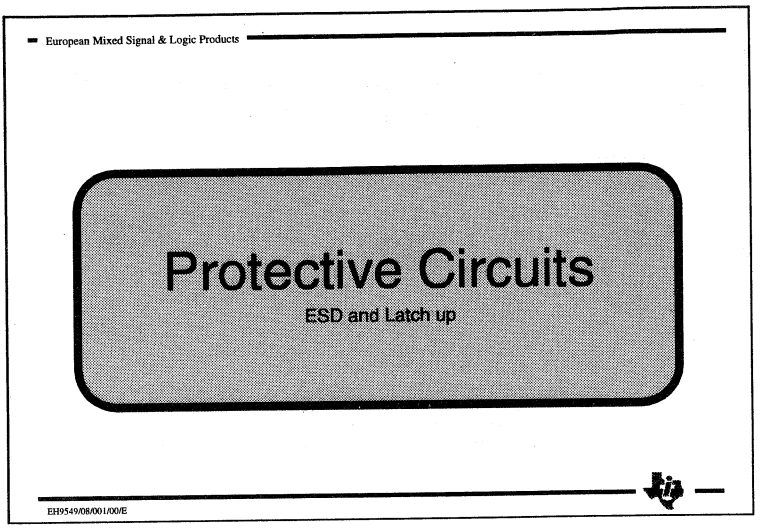
To analyse the characteristic of transmission lines therefore a random pattern bit stream has to be applied to the input of the cable while observing the response at the end of the lines. A pseudo random pattern generator can be made easily by a shift register with a feedback from some of the outputs to the serial inputs via an Exclusive OR function. When selecting the correct feedback path the repetition period of this generator is 2^n-1 shift clock cycles, where n is number of bits in the shift register. The picture above shows such a pseudo ransom pattern generator with an 8-bit shift register. The repetition period in this examples is 2^8-1 = 255 shift clock cycle.



Eye Pattern (14030)

Using the pseudo random pattern generator described above, the transfer characteristic of a twisted pair cable has been tested. The cable has length l = 1000 m and wire diameter d = 0.6 mm. The data rate is r ≈ 300 kBit/s (bit duration ≈ 3.5 s). The signal at the beginning (upper trace in the above picture) is a square wave. At the line end the low-pass filter performed by the cable slows down the rise time as well as the amplitude (lower trace). The ohmic resistance of the wire has only a minor influence when comparing the peak voltages at the beginning and the end of the line.

The majority of the signal quality degradation is caused by the frequency-dependent losses (skin effect). The voltage swing and the time interval left for recovering the transmitted information is the eye-shaped window in the signal flow. The height of the window gives the effective signal amplitude which has to be detected by the receiver circuit. The width of the eye determines the final time interval in which the information has to be sampled. This picture shows also that the point of transition between the single bits varies depending on the previous bit sequence. This transition time variation is called jitter. Therefore in many receiver systems one can find a sophisticated clock recovery circuit to regenerate the original timing (clock) of the information for correct sampling of the data.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ESD and Latch up
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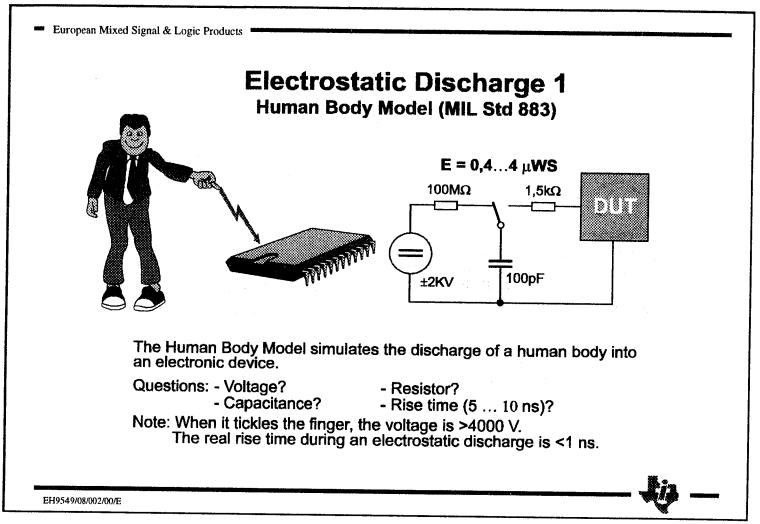


Electrostatic Discharge 1, Human Body Model (08002)

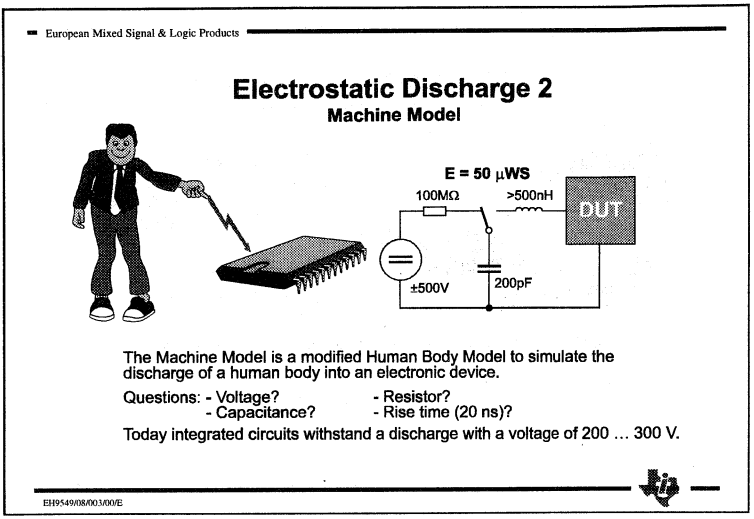
Various test methods have been developed to analyse the immunity of electronic components to damage by an electrostatic discharge. One popular test circuit is the so-called Human Body Model, which simulates the situation where the electric charge stored in a human body is discharged into the device under test. To simulate that a capacitor C = 100 pF (capacitance of the human body) is charged up to a voltage of V = ±2000 V and is discharged thereafter via a resistor R = 1.5 kΩ into the circuit. Despite the question as to how far this test circuit really simulates the situation mentioned some comments are necessary to explain the different modes of destruction:

1) Short transition time of the discharge: The transition time of the current in the circuit under test at the beginning of the discharge is extremely short: $t_r < 1$ ns. During this short time interval only a small area of the total protection network inside the integrated circuit starts to conduct. This small area in some cases is not capable of dissipating the total power. The silicon melts and the device is destroyed. This phenomenon explains also that if the discharge does not occur in immediate neighbourhood of the circuit but at a certain distance the device will survive: the inductance of the interconnect between the point of discharge and the integrated circuit slows down the rise time. Now the total area of the integrated protection network can conduct and short the current to ground.

2) High current: The protection network must be able to carry the relative high currents during the discharge. In the test circuit shown above the peak current is ≈1.5 A.

3) High energy: The protection network must capable to handle the energy during a discharge. Mostly however the energy is not of concern. Most of the power stored in the capacitor is dissipated in the series resistor. Assuming the breakdown voltage of the device under test to be V_{br} = 20 V (in most applications only the forward voltage of the clamping diode V_f = 1 to 2 V has to be considered), the resulting Energy E_a to be absorbed by the device under test can be calculated as follows:

$$E_a = V_{br} \cdot V \cdot C = 20V \cdot 2000V \cdot 100pF = 4\mu Ws$$



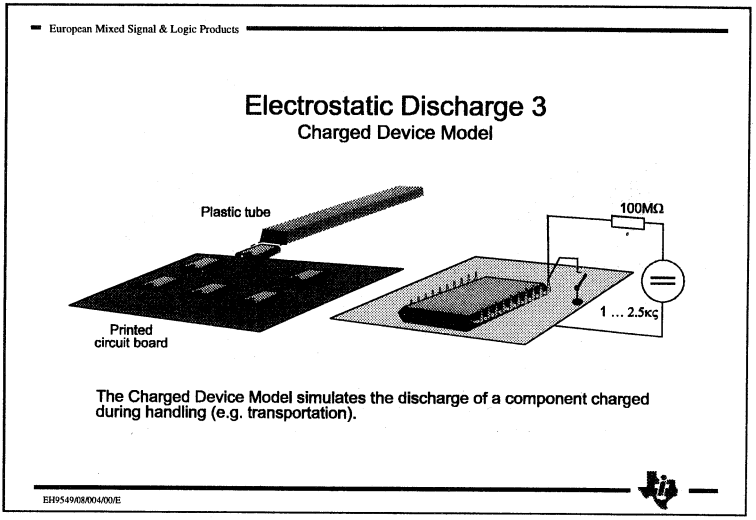
Electrostatic Discharge 2, Machine Model (08003)

Another test circuit had been developed in Japan called the Machine Model. In this test set up a capacitor of C = 200 pF is charges up to a voltage V = ±500 V, thereafter the capacitor is discharged into the device under test without any current limiting series resistor. Because of this, the energy Ea to be absorbed in the device under test becomes much larger:

$$E_a = 0.5 \cdot V^2 \cdot C = 500^2 V^2 \cdot 200 pF = 50 \mu Ws$$

On the other hand, the test specification allows a relatively high inductance in the discharge circuit (up to 500 nH). This inductance slows down the rise time of the discharge current. Finally, this test mostly addresses the capability of the device under test to absorb a certain amount of energy. That a fast reaction time of the protection circuit is required for fast slew rates is not so much of concern.

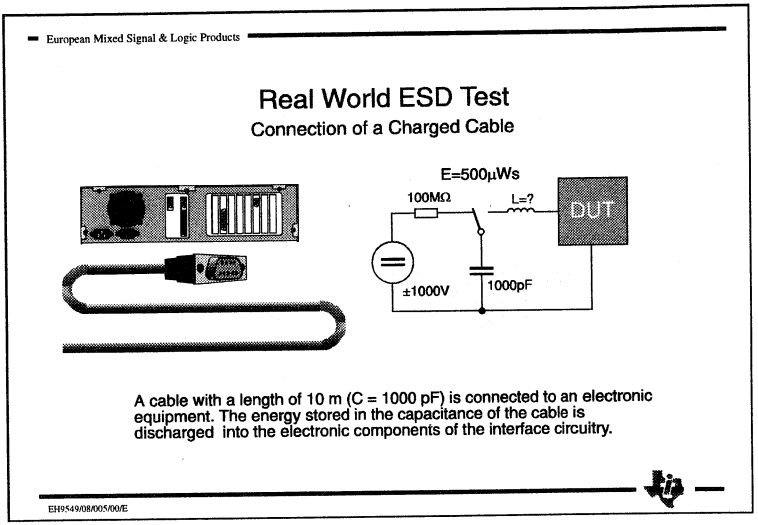
Last but not least, state-of-the-art integrated circuits withstand without damage a Human Body Model (2000 V; 200 pF; 1.5 kΩ), while most circuits in a Machine-Model test, they withstand only voltages up to 200...300 V.



Electrostatic Discharge 3, Charged Device Model (08004)

Even after continuos improvement of the capability of protection networks inside integrated circuits, damaged components were still found after assembly on a printed board. A detailed investigation showed that this destruction could be explained by the following situation: In an automatic assembly equipment during assembly the integrated circuit in question slides through the plastic tube (the container during transportation and storage) and is charged up. When the circuit lands on the printed circuit board the capacitance of the device is discharged again. By this discharge, the circuit may be destroyed.

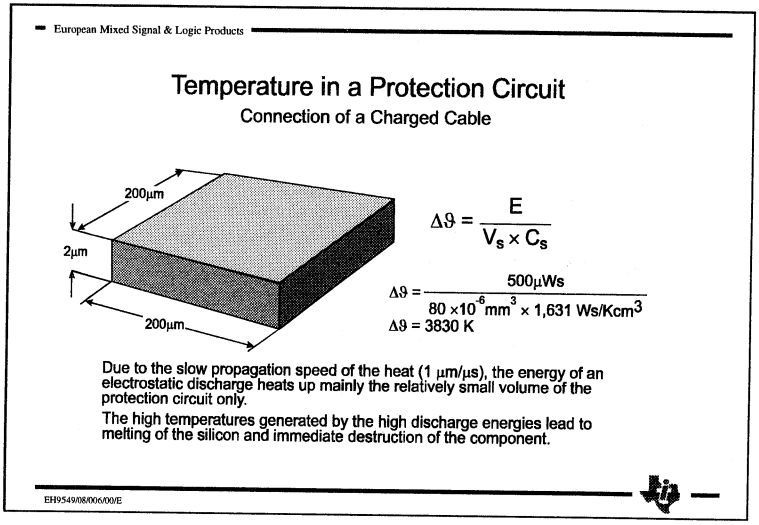
To test the immunity against discharge the device under test is placed on a metal plate (see the above figure). The circuit is charged up to a voltage V = 1,5 to 2 kV. Thereafter the pin of the device to be investigated is shorted to the metal plate. It has been demonstrated that integrated circuits which withstand a test with a voltage V = 1,5 to 2 kV, are not degraded during the assembly cycle. Circuits which withstand a lower voltage, may be degraded. It has to be mentioned that until now no correlation has been found between the test results of the human body model test and the charged device model test. Circuits which show a good performance in one test environment, may fail in the other one.



Real World ESD Test (08005)

All the tests shown above by far do not show the rough treatment which may happen to interface circuits. At typical situation is the following: A modem needs to be connected to a personal computer. The modem is placed at one end of the room, the computer at the other end, with 10 m between these two equipments. The man who installs the cable walks through the room over carpet, which as is well-known, generates high electrostatic charge. By keeping one end of the cable in his hand, the cable may be charged up to a voltage V = 1000 V. When the cable is now connected to the equipment, the capacitance of the cable C = 1000 pF is discharged into the interface circuits. The energy to be absorbed under this condition is far higher than that found in the previous test standards:

$$E_a = 0.5 \cdot V^2 \cdot C = 0.5 \cdot 1000^2 V^2 \cdot 1000 pF = 500 \mu Ws$$

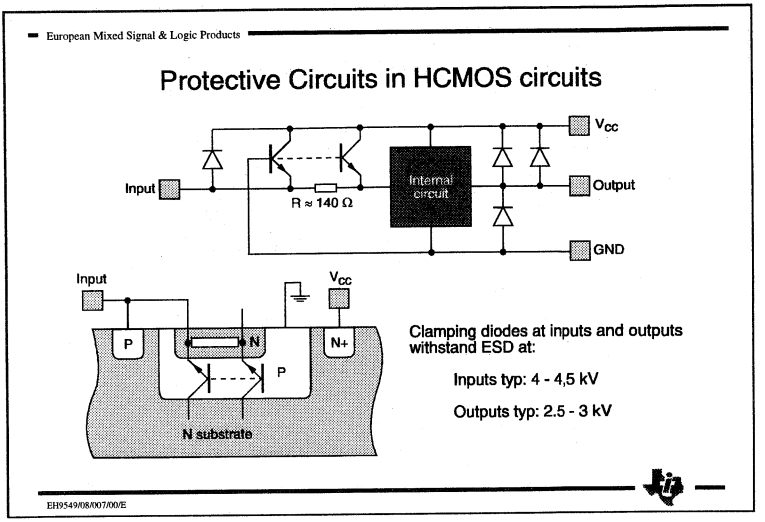


Temperature in a protection circuit (08006)

The protection network inside an integrated circuit has to absorb the energy during the electrostatic discharge described above. The discharge time is relatively short. In the case of the charged cable the discharge time is twice the propagation time of a wave on the cable = 2 × 10 m × 5 ns/m = 50 ns. During this time energy is injected into the protection circuit. It is further assumed that the protection circuit occupies an area of 200 × 200 mm^2 (four times the size of a bond pad), and that the depth of the junction is 2 µm, which results in a volume V_s = 80 × 10^{-6} mm^3. Considering, that the thermal propagation time of the heat wave in the silicon crystal is about 1 µm/µs., one can say that during the first microseconds the total heat will stay in the protection circuit. By knowing the thermal capacitance of silicon C_s = 1.631 Ws/Kcm3, the temperature increase $\Delta\vartheta$ in the protection network can be calculated:

$$\Delta\vartheta = \frac{E_a}{V_s \cdot C_s} = \frac{500\mu Ws}{80 \cdot 10^{-6} mm^3 \cdot 1.631 Ws/Kcm^3} = 3830K$$

The melting temperature of silicon is about 1600°C. The aluminium metallization - already melted at much lower temperatures - will diffuse into the silicon. The normally high impedance ESD protection circuit becomes a short circuit.

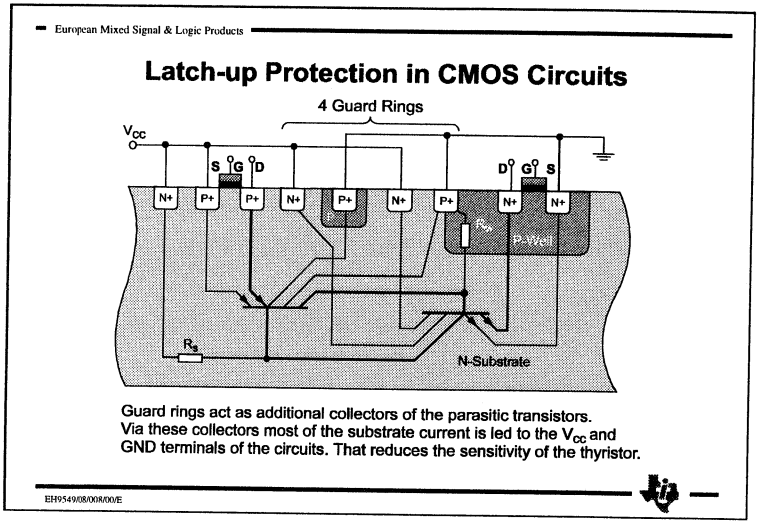


Protective Circuits in HCMOS Circuits (08007)

The protection circuits in integrated components are of different kinds depending on the actual requirements. Bipolar integrated logic circuits for example in most cases do not require any special measures at the outputs due to the high current capability of the output transistors. These components already guarantee sufficient protection against damage by an electrostatic discharge. In CMOS circuits additional measures are required. At the output we find diodes to the positive (V_{cc}) and negative (GND) supply rails, which in a case of a discharge lead the current to these supply rails. A second diode shown at the output and the Vcc terminal is a so called parasitic diode generated by the p-doped diffusion of the drain of the output transistor located in the n-doped substrate.

At the inputs of CMOS circuits we mostly find diodes to the V_{cc} rail to limit positive voltages. The limiter for negative voltages in the above circuits diagram looks like a transistor with a resistor in parallel. The original design goal was a resistor - to limit the current - and a diode - to limit the voltage -. The result is shown in the picture above: The resistor is an n-doped diffusion area placed in a p-doped tank (for isolation purpose). The total circuit again is located in a n-doped substrate. Beside the desired resistor and diode this structure also produces a so-called parasitic PNP transistor. In the case of the protection circuit this will not be any disadvantage. During an electrostatic discharge a certain amount of the current will flow via the parasitic collector also to the V_{cc} rail. That however will not degrade the quality of the circuit.

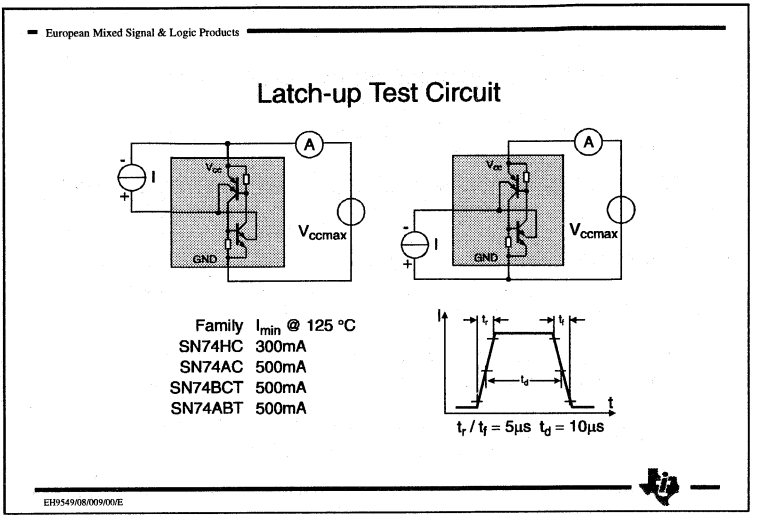
The circuit described here shall be an example only. In practice one finds a wide variety of circuits adapted to the application requirements as well to the process capabilities of the semiconductor structure.



Latch up Protection in CMOS Circuits (08008)

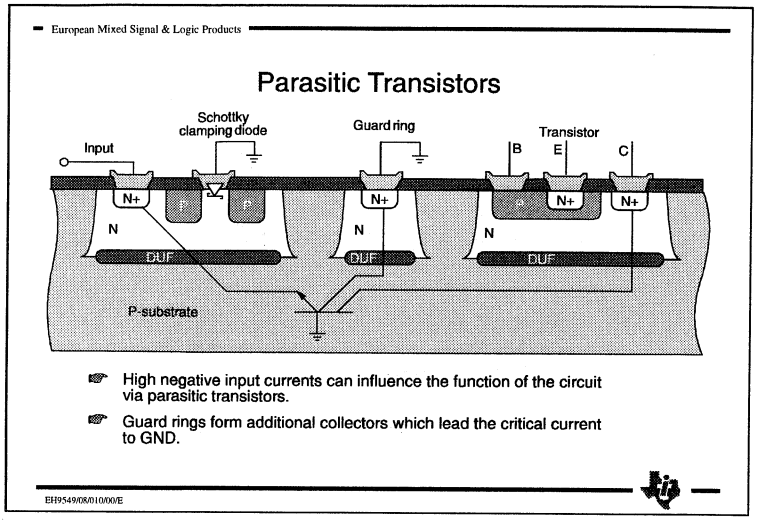
Whenever a semiconductor manufacturer produces complementary MOS circuits (CMOS), PNPN structures are generated on the silicon chip. In the above picture the p-diffusion of drain and source of the p-channel transistor are located in an n-doped substrate. The n-doped source and drain of the n-channel transistor are placed in a p-doped well for isolation purpose. This well is again located in the substrate. This arrangement acts as a thyristor where the anode and the cathode are connected to the supply terminals of the circuits, while all inputs and outputs are the gates of the thyristor. By driving a sufficient current into any input or output the thyristor will be fired causing a short circuit between the supply terminals (latch-up). This overload will immediately destroy the integrated circuit.

To avoid latch-up semiconductor manufacturers place guards rings inside the integrated circuits. These p- or n-doped areas connected to the positive and negative supply rails respectively surround the critical parts of the circuits. They provide additional collectors for the parasitic transistors which short most of the current which may fire the thyristor to the supply rails. This technique reduces the sensitivity of the thyristor in such way that under normal operation latch-up will be avoided.



Latch up Test (08010)

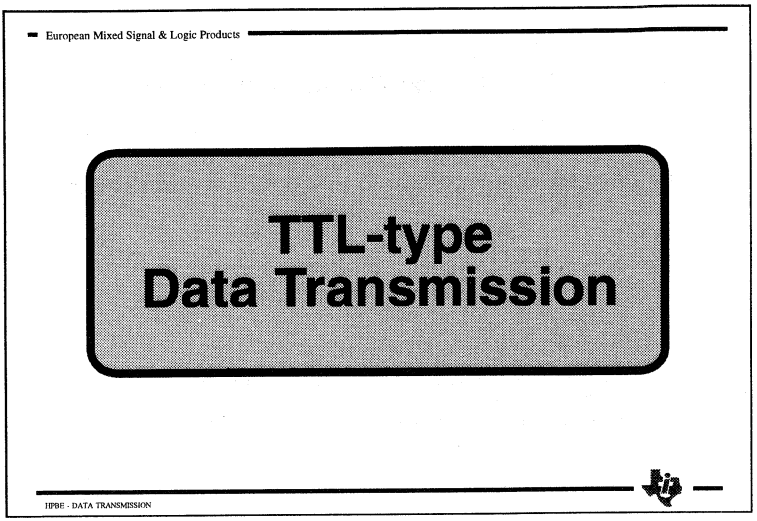
During the characterisation process of an integrated circuit a latch-up test is also performed, to check the efficiency of the protection circuits. For this purpose a high positive and negative current is driven into any input or output terminal of the integrated circuit to check if there is any way to fire the thyristor and to cause latch-up. The current pulse in this test has to have a certain length (several microseconds) since the transit frequency of the parasitic transistors is very low ($f_t \approx 1$ MHz). A very short pulse is thus hardly able to generate latch-up. Note, that this test is a destructive test. The test is performed at $T_a = 125°C$ since the current gain of the parasitic transistors, and thus the sensitivity the thyristor increases with temperature. As the table above shows, currents of the order of several 100 milliamperes will not cause latch-up. Therefore in practice state-of-the-art integrated CMOS circuits are immune against latch-up.



Parasitic transistors (08010)

The picture above shows the structure of a typical bipolar integrated circuit. On the left side is found the Schottky clamping diode (n-metal junction). This diode limits negative undershoots caused by line reflections. With low negative input currents at this diode the forward voltage of this diode is about 0.5 V. With increasing current the forward voltage of the diode also increases. At a certain current amplitude the forward voltage of the diode becomes higher than 700 mV. At this point the n-p junction to the substrate also starts to conduct. This n-p junction is the base emitter diode of a parasitic transistor, while all n-doped areas in the neighbourhood are the collectors of the parasitic transistors. With a sufficiently high current into the clamping diode and the substrate the parasitic transistor will be turned on. By this the collector of the transistor in the right side in the picture above is pulled to a low level. Due to this undesired effect, the integrated circuit may not function correctly, again.

To avoid these parasitic effects, guard rings are again placed around the input circuitry - in this case the clamping diode. These guard rings perform as an additional collector of the parasitic transistor which shorts most of the current in the substrate to ground. This technique again does not eliminate the parasitic transistor, but it reduces its current gain so far, that under normal operating conditions no malfunction of the integrated circuit will occur. For example, the guard rings of logic circuit of the series SN74xx are designed so that a negative input current I_{il} = -60 mA for a duration t_d = 100 ns will not cause a malfunction of the integrated circuit.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TTL-type
Data Transmission
IIPBE - DATA TRANSMISSION

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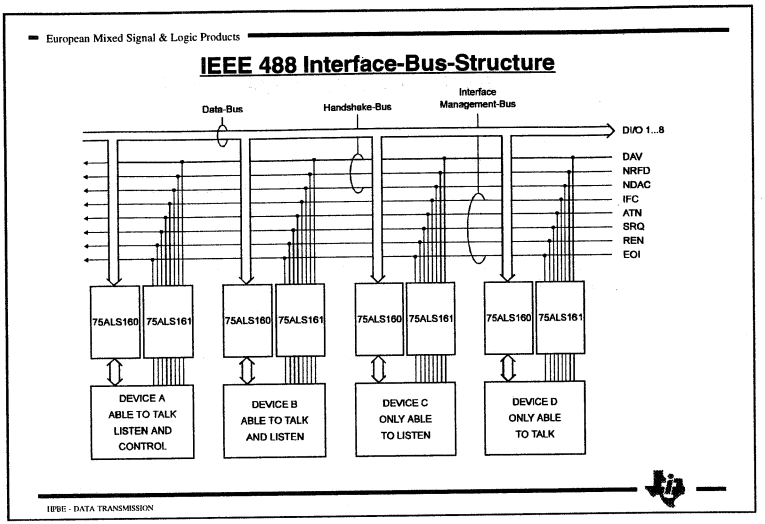
IEEE 488 - General Purpose Interface Bus (GPIB)

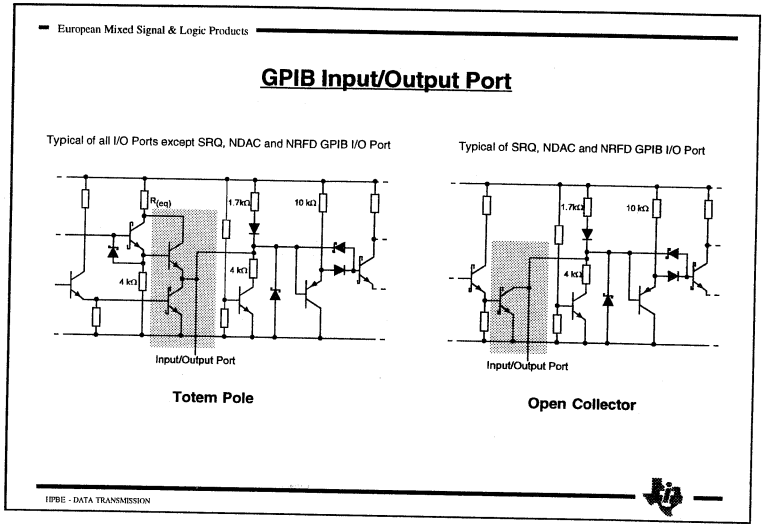
- The IEEE 488 specification describes an universal interface bus, which consists of 8 parallel control lines and 8 parallel data lines.
- This interface is used for communication between a processor and programmable measurement and similar equipment.
- The 8 bit parallel data bus works with a data rate of max. 1.5 MByte/s



IEEE 488 Interface-Bus-Structure

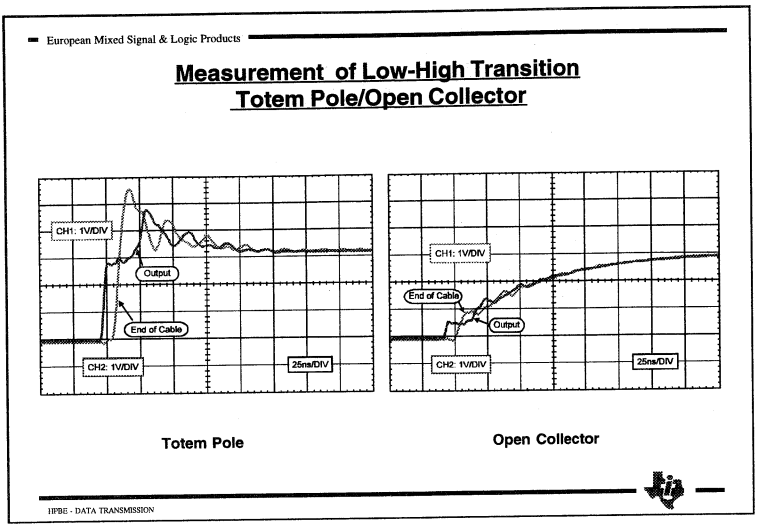
The figure illustrates a typical application of a complex GPIB system. The figure shows the 8 bit data-bus and the 8 bit control bus. Texas Instruments offers in the SN75ALS16x family several transceivers, that meet the IEEE 488 standard.

Careful attention must be paid to the 8 signal lines DAV, NRFD, NDAC, IFC, ATN, REN, and SRQ. Each of the signal line must be twisted with one of the logic ground wires to minimize crosstalk.



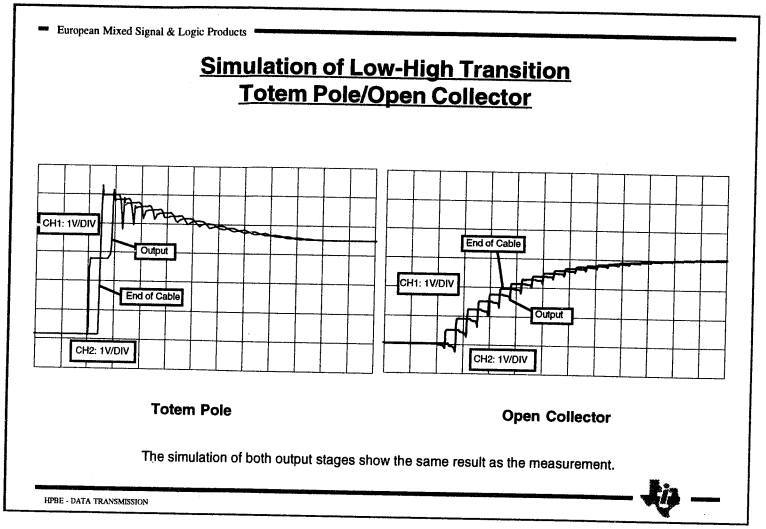
GPIB Input/Output Port

The typical input/output stages are illustrated in this figure. Outputs are either totem pole or open collector. A totem pole output is required for faster data rates. Open collector outputs must be used, if parallel polling is required (wired-and, wired-or function with multiple lines). The output stages SRQ, NDAC and NRFD are configured as open-collector output stages. All driver outputs feature active bus-terminating resistor circuits, designed to provide high impedance to the bus when Vcc = 0V. The input stages are similar. Each of the inputs consists of a clamping diode to limit the negative undershoots at the end of the line. A further termination is therefore not required.



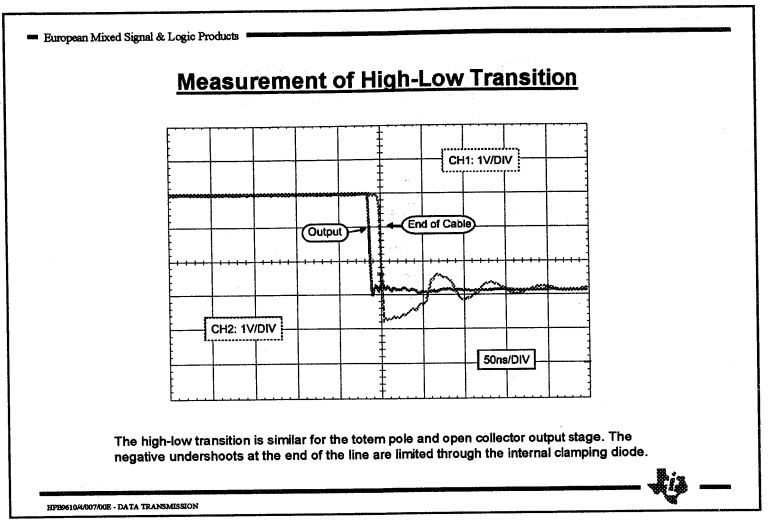
Measurement of Low-High Transition Totem Pole/Open Collector

The figures show the low-high transition of the totem pole and open collector output stage. It is obvious that due to the misterminated line the low-high transition of the open collector output stage is substantial slower than the low-high transition of the totem pole output. The energy to charge the capacitance of the line has to be provided via the high impedance resistor network in the bus interface circuits.



Simulation of Low-High Transition Totem Pole/ Open Collector

The simulation of both output stages show the same result as the measurement.



Measurement of High-Low Transition

The high-low transition is similar for the totem pole and open collector output stage, because the output impedance in the low case of the open collector- and of the totem pole output stage are the same. The negative undershoots at the end of the line are limited through the internal clamping diode. A further clamping diode is therefore not required.

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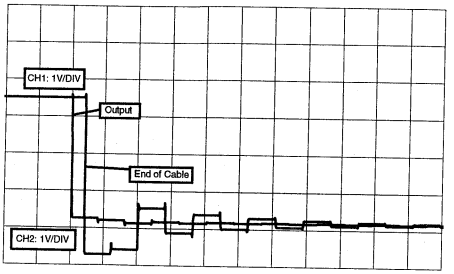
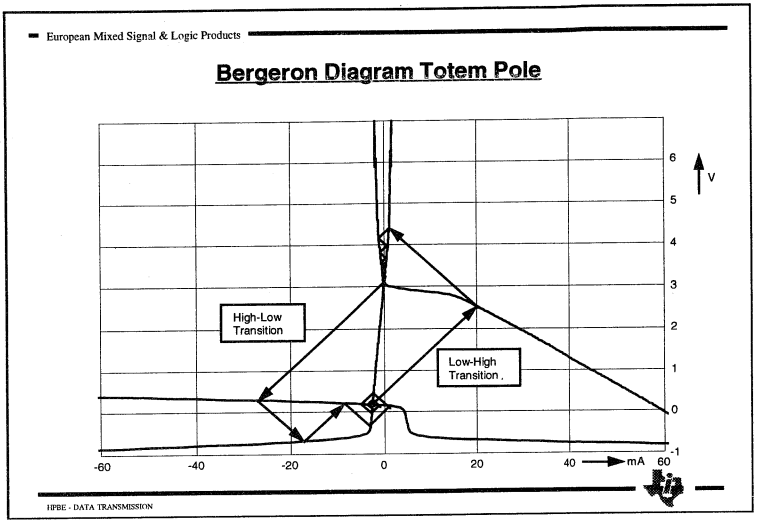
Simulation of High-Low Transition

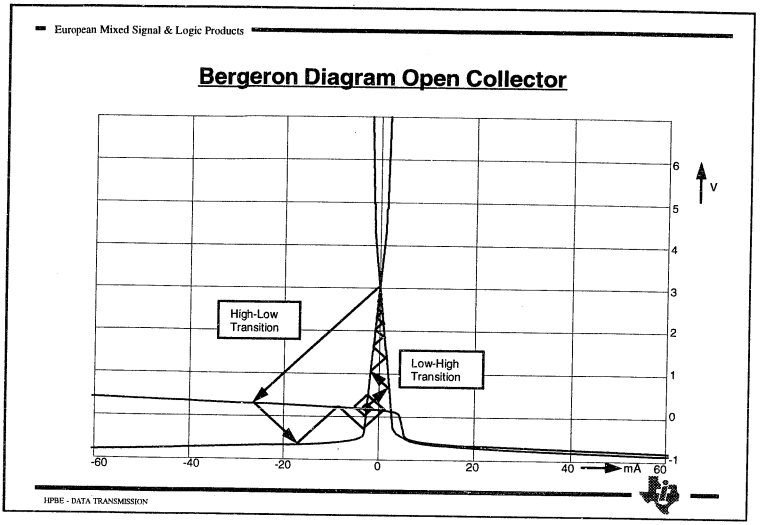


The simulation of the high-low transition confirms the measurement.



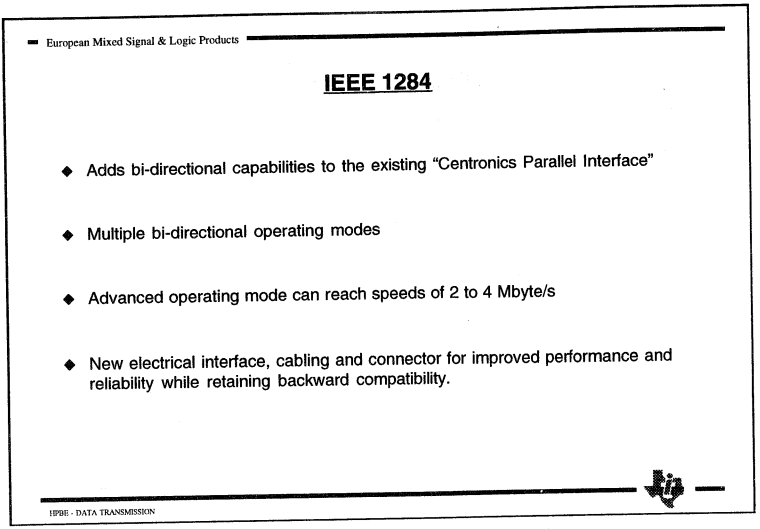
Bergeron Diagram Totem Pole

As already mentioned in the section 'Basics and Practical Examples of Transmission', the Bergeron Diagram is a simple tool to analyse line reflections in circuits which show nonlinear characteristics as in semiconductor components. The picture above shows the Bergeron Diagram for the totem-pole output stage with its voltage/current diagram, the output characteristic of the driver for the low and high case, and the input characteristic of the receiver. The drawing lines with the alternating slopes show the voltages at the end and at the beginning of the line. The Bergeron Diagram confirms the results of the measurement and simulation.



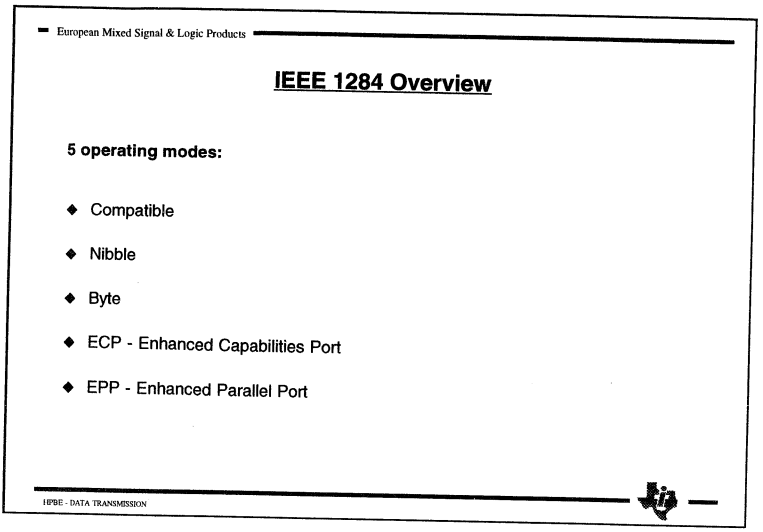
Bergeron Diagram Open Collector

The Bergeron Diagram confirms that the low-high transition of the open collector output stage is very slow.



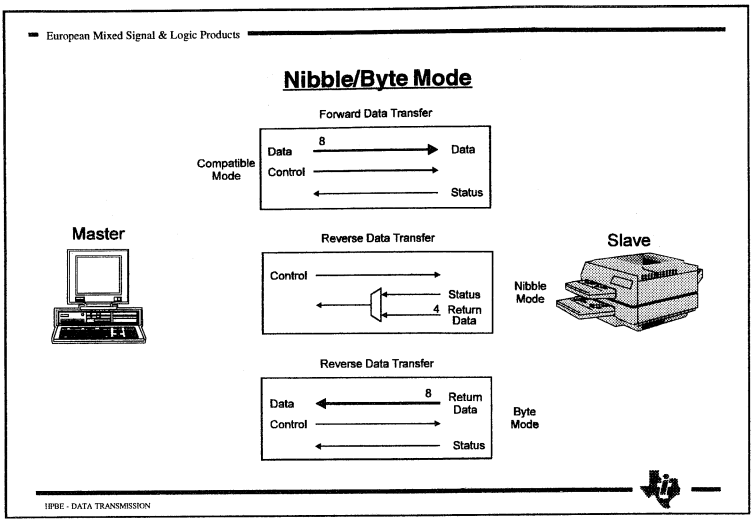
IEEE 1284

The IEEE 1284 standard, "Standard Signaling Method for a Bi-directional Parallel Peripheral Interface for Personal Computers" was created because there existed no defined standard for bidirectional parallel communications between personal computers and peripherals. Pre-existing methods used a wide variety of hardware and software products, each with unique and incompatible signaling schemes. This standard was developed to provide an open path for communications between computers and more intelligent printers and peripherals.



IEEE 1284 Overview

The interface supports a number of distinct communication modes. The following figures give a brief description of the different modes.



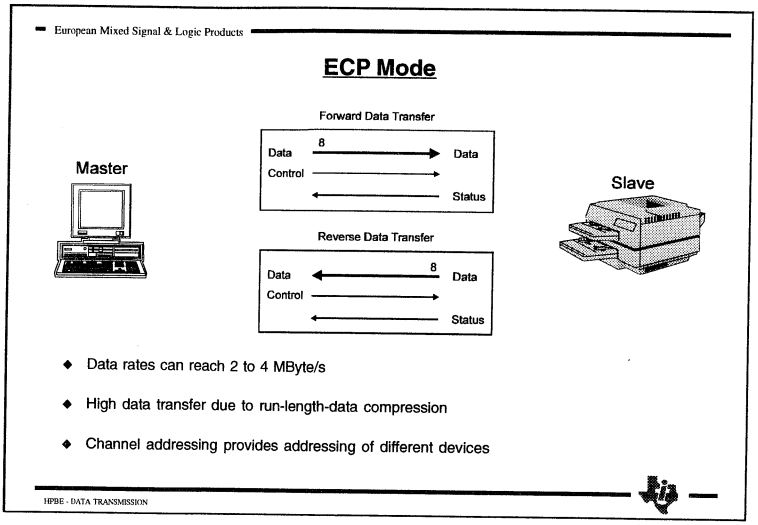
Nibble/Byte Mode

The Compatibility Mode provides host to peripheral communications in a manner compatible with the traditional uni-directional interface.

In the Nibble and Byte Modes of operation, data from the host to printer is sent using the compatibility mode of operation. Data is sent over the 8 data lines in parallel. The reverse data transfer, peripheral to host, can be achieved in one of two ways.; either 4 bits, a nibble at a time, or 8 bits, a byte at a time. In the Nibble Mode, transfer of data from the printer to the host is accomplished using 4 of the printer status lines. The advantage of the nibble mode is that data transfer can be functionally implemented totally in a software driver on the installed base of personal computers.

In the Byte Mode the reverse data transfer is by the 8 data lines defined for forward transfer of data. This method is again compatible with personal computers that provide the 8 bit reverse data path capability such as the IBM PS/2 machines.

In these modes of bi-directional communication, the host is the master of the system and in complete control of the direction of the data link.

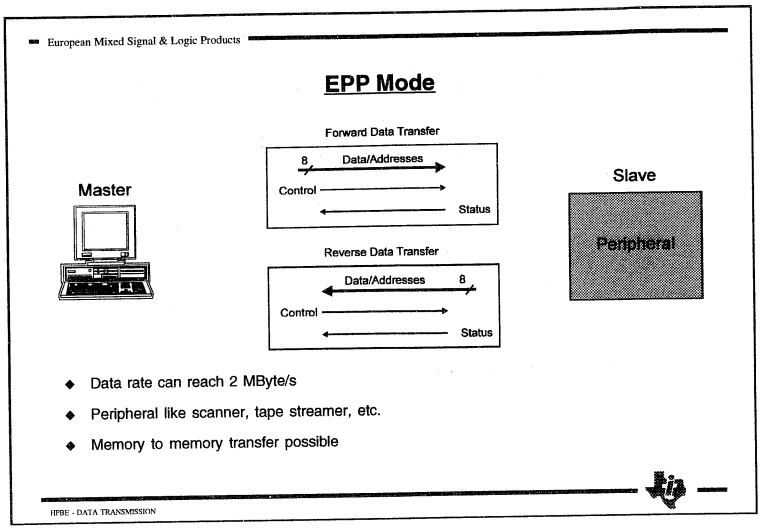


ECP Mode

The Enhanced Capabilities Port Mode of operation provides symmetric bi-directional communications without the overhead of changing the communication modes.

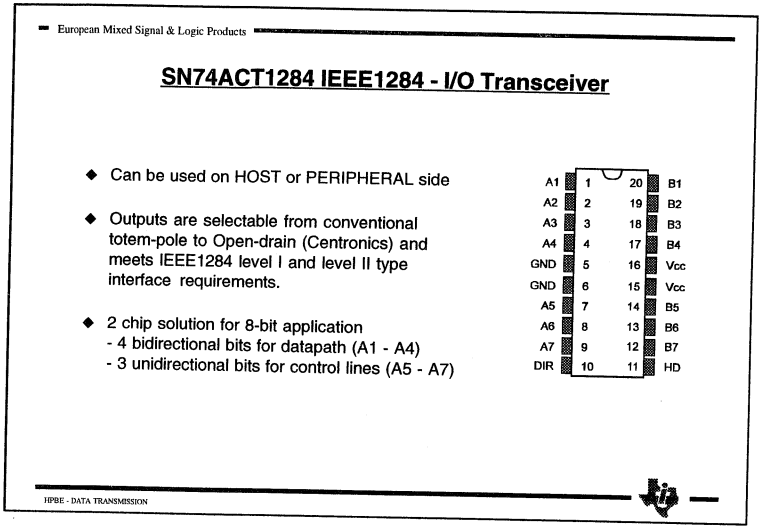
Data can be transferred between the two systems, 8 bits, at a time in a half duplex fashion. Data rates can reach 2 to 4 megabytes per second.

The ECP Mode is capable of higher operating rates at speeds of 2 to 4 Mbps in a half duplex fashion. The mode will require new hardware capabilities and is intended to be used in new designs of host computers.



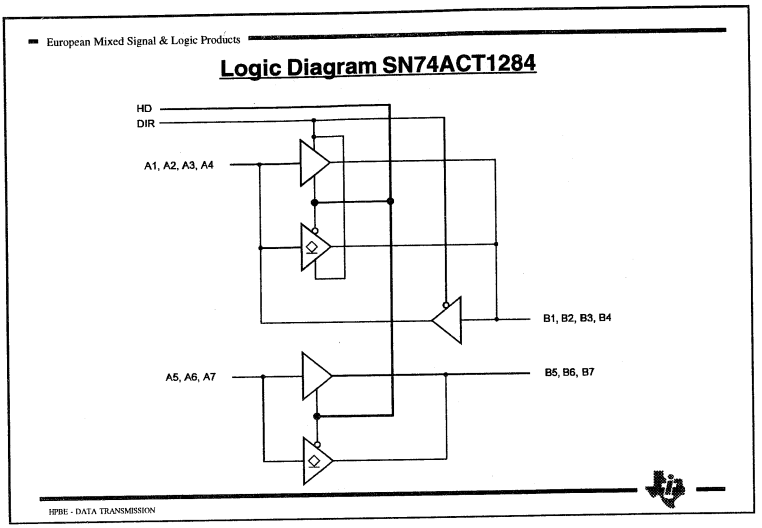
EPP Mode

The Enhanced Parallel Port, EPP Mode provides a half duplex bi-directional data transfer driven by the host device. The data rate can reach up to 2 Mbps. The EPP is primarily used by non-printer peripherals, CD-ROM, tape, hard drive, network adapters, etc.



SN74ACT1284 IEEE 1284 - I/O Transceiver

The SN74ACT1284 allows the printer or other peripheral to be connected to the host PC while the system is active. This live insertion capability is needed to support the plug-and-play initiative supported by current systems, such as Microsoft Windows™ 95. The SN74ACT1284 provides a reliable transfer of data over cables of up to 10 meters in length and at speeds up to two megabytes per second.



Logic Diagram SN74ACT1284

Since some systems must remain backward compatible with the older Centronics standard interface, the SN74ACT1284's outputs can be switched from its normal totem-pole output to an open-drain output. The output drive for each mode is determined by the high drive (HD) control pin. When HD is high, the high drive is delivered by the totem-pole configuration, and when HD is low, the outputs are open-drain. This meets the drive requirements as specified in the IEEE 1284-I (level 1 type) and the IEEE 1284-II (level 2 type) parallel peripheral specification.

Furthermore the device allows data transmission in either the A-to-B or the B-to-A direction for bits 1, 2, 3, and 4, depending on the logic level at the direction control (DIR) input. Bits 5, 6, and 7, however, always transmit in the A-to-B direction.

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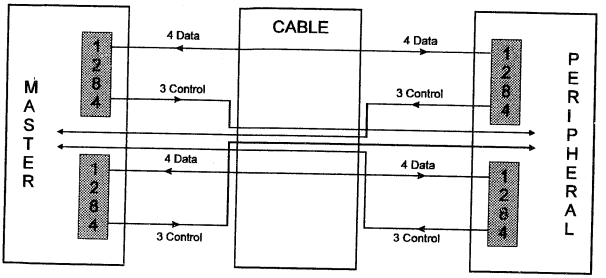
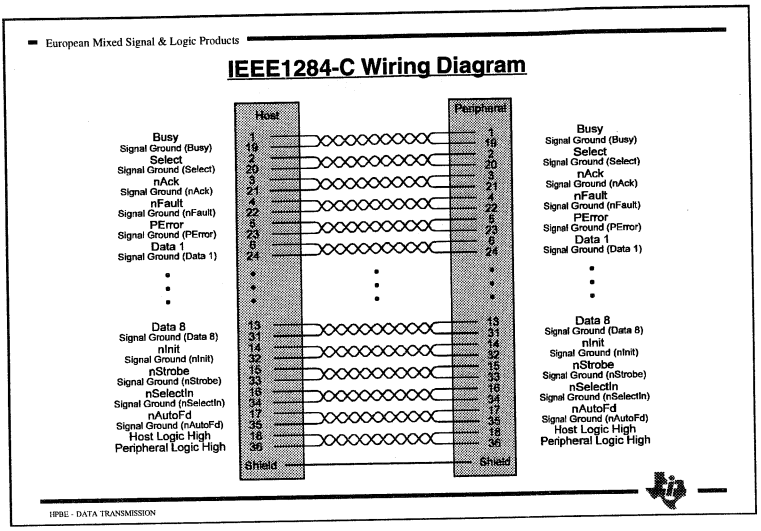
SN74ACT1284 Application



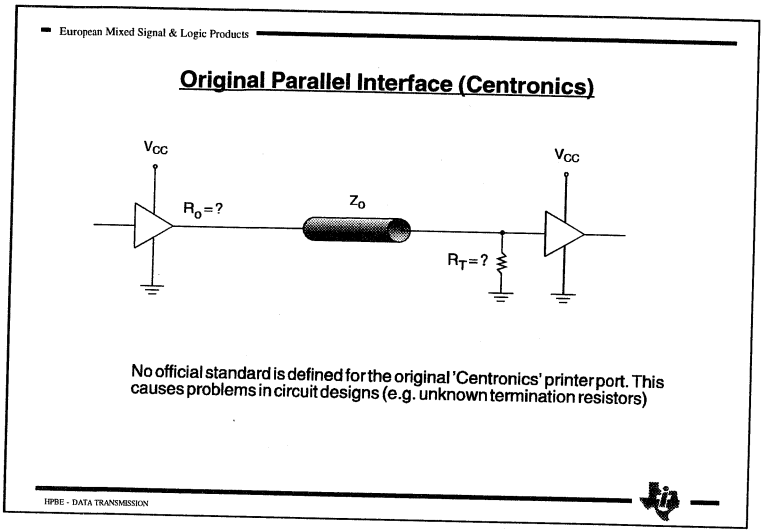
- Bidirectional datapaths allow application on HOST or PERIPHERAL side
- Controlled edge rate outputs reduces transmission line effects on cable
- Open-drain selectable outputs allow 'Centronics' type peripheral interface

HPBE - DATA TRANSMISSION



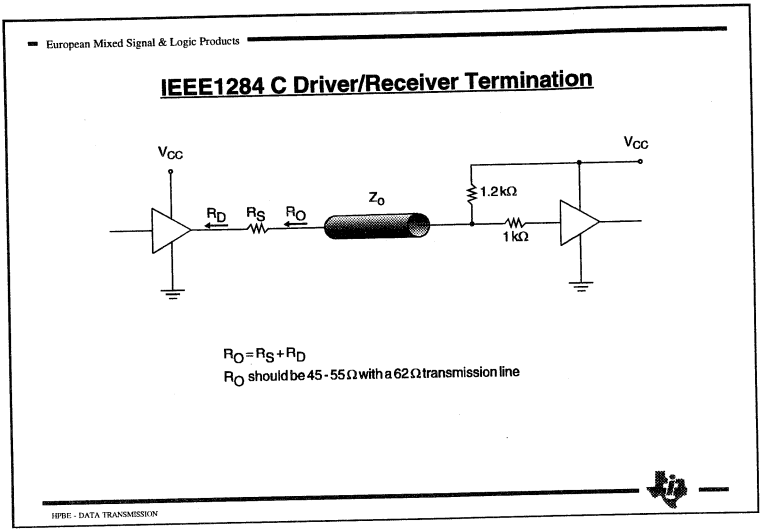
IEEE 1284-C Wiring Diagram

The picture above shows the IEEE 1284-C (host) to IEEE 1284-C (peripheral) wiring diagram. It can be seen that each signal line should be twisted with Signal Ground to minimize the crosstalk and to achieve a high data rate.



Original Parallel Interface (Centronics)

An official standard has never been defined for the original 'Centronics' printer port. This causes problems in circuit designs, because of unkown hardware design elements, such as termination resistors or driver output impedances. Therefore for safe data transmission, only a short cable between host and peripheral (1 to 2 m) is allowed.



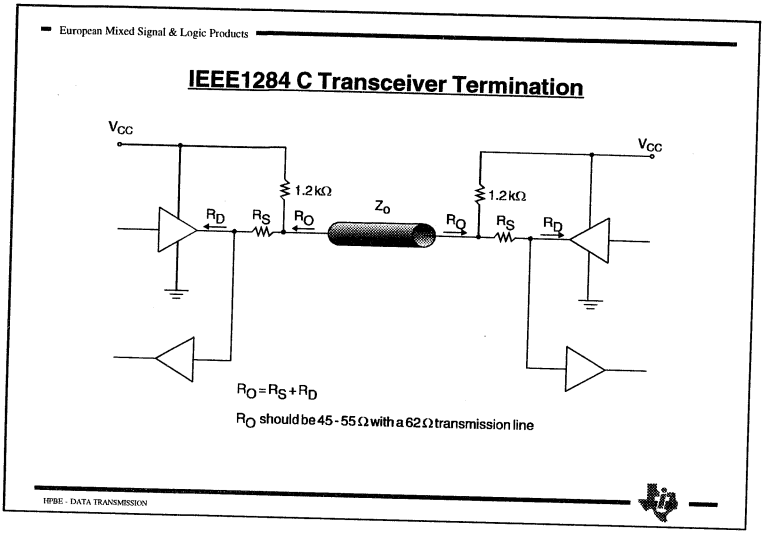
IEEE 1284 C Driver/Receiver Termination

The intent of the termination is to match the characteristic impedance at the source and have a high impedance at the load. This will cause half the source voltage to be injected into the cable and a doubling of voltage at the load. Because of component tolerance, the matching source impedance is slightly lower than the nominal characteristic impedance of the cable to guarantee proper voltage levels at the load.

Referring to the figure, R_D is the output impedance of the circuitry of the active driver. R_S is a series resistor used for matching. R_0 represents the combined output impedance of the driver and impedance matching resistor (the sum of R_S and R_D). R_0 should be 45-55Ω. This causes the driver to generate an incident wave of amplitude slightly in excess of one-half V_{OH} minus V_{OL}, into an infinitely long 62Ω transmission line as measured at the driver/cable interface, for transitions in either direction.

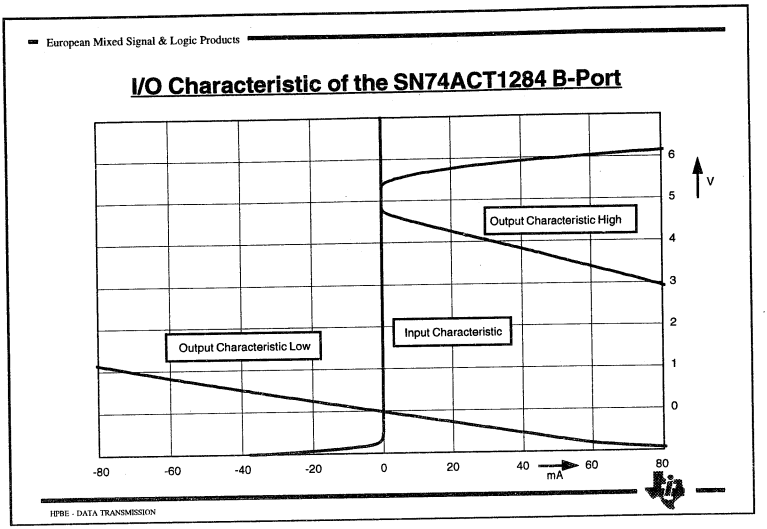
All input signals provide pullup resistors to + 5V to ensure operation with Level 1 and compatible devices.

The 1kΩ resistor in series of the receiver input is recommended for ESD protection.



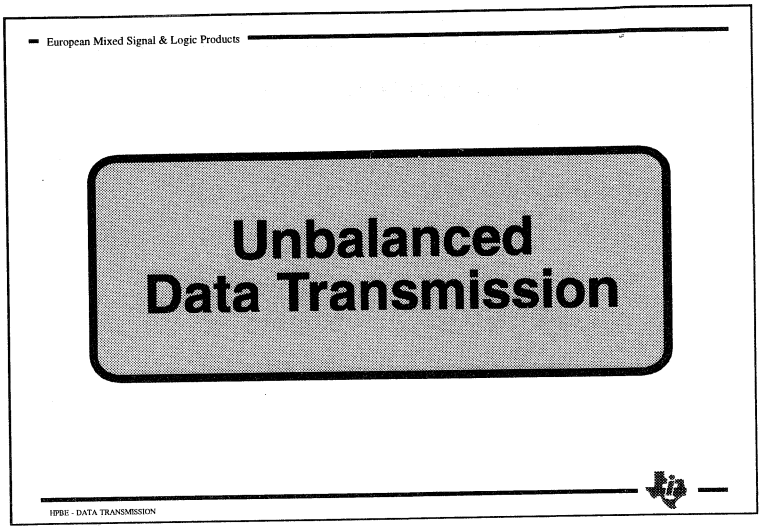
IEEE 1284 C Transceiver Termination

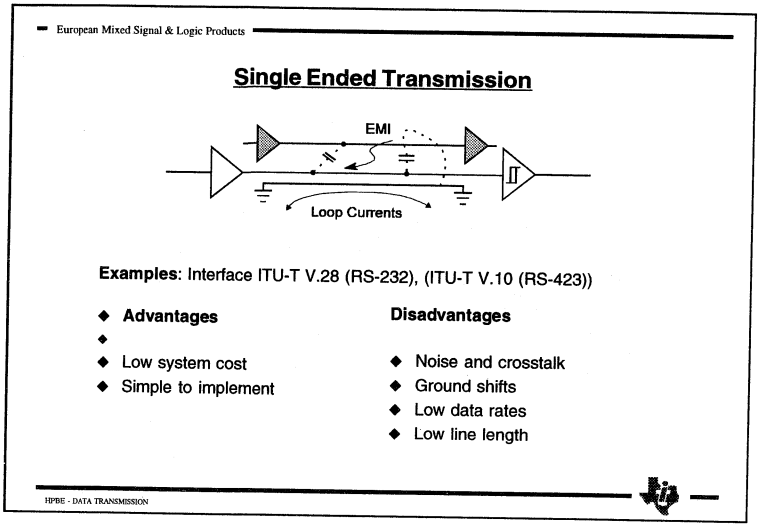
The IEEE 1284 transceiver termination is in principle similar to the driver/receiver termination. However, in this termination it is not possible to implement the 1kΩ resistor in series for ESD protection of the receiver input, without having a mismatching at the driver output.



I/O Characteristic of the SN74ACT1284 B-Port

The I/O characteristic of the SN74ACT184 B-Port is shown in the figure above. It gives an indication of the actual behavior of the component in a system and is also useful to predict the waveforms (Bergeron Diagram, Lattice Diagram) resulting from line reflections.


European Mixed Signal & Logic Products
Unbalanced
Data Transmission
HPBE - DATA TRANSMISSION



Advantages of single ended transmission

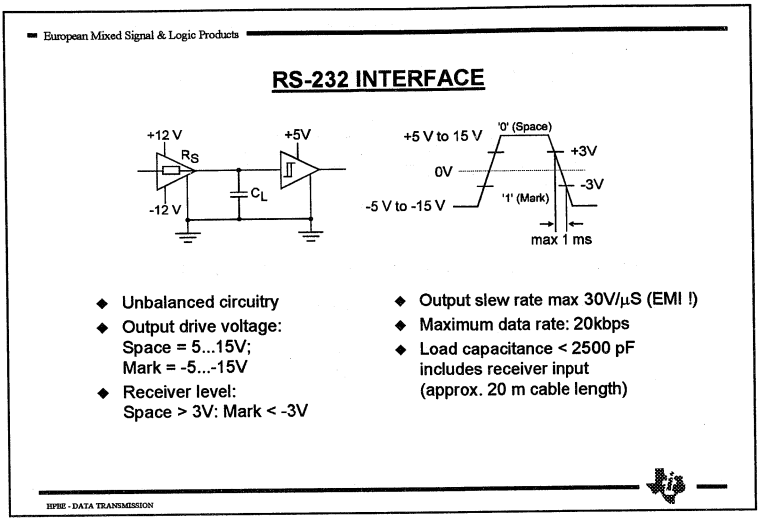
The advantages of single ended transmission are simplicity and low cost of implementation. Obviously a single ended system requires one line per signal and is therefore ideal for parallel communication where many lines are required e.g. PC parallel printer port or serial communication with many handshaking lines e.g. EIA-232. Cabling costs can be kept to an absolute minimum with short distance communication requiring no more than a low cost ribbon cable. For longer distances or/and noisy environments, shielding is essential and cabling costs begin to increase.

Disadvantages of single ended transmission

The main disadvantage of the single ended solution is its poor noise immunity. Because the ground wire forms part of the system, transient voltages or shifts in voltage potential may be induced (from nearby high frequency logic or high current power circuits), leading to signal degradation. This ultimately leads to false receiver triggering. For example, a shift in the ground potential at the receiver end of the system can lead to an apparent change in the input switching threshold of the receiver device, thus increasing its susceptibility to noise.

Cross talk is also a major concern especially at high frequencies. Cross talk is generated from both capacitive and inductive coupling. Capacitive coupling tends to be more severe at higher signal frequencies as capacitive reactance decreases. The impedance and termination of the coupled line determines whether the electric or the magnetic coupling is dominant. If the impedance of the line is high the capacitive pickup is large. Alternatively, if the line impedance is low, the series impedance as seen by the induced voltage is low, allowing large induced currents to flow.

These problems will normally limit the distance and speed of reliable operation for a single ended link.



EIA-232 Specification

All circuits in accordance to EIA-232 carry bipolar voltage signals which must not exceed +/- 25V at the connector pins. Any pin must be able to withstand short circuit to any other pin without sustaining permanent damage. Each line should have a minimum load of 3 kΩ and maximum load of 7 kΩ which is usually part of the receiver circuit. A logic '0' is represent by a driven voltage of between +5 V and +15 V and a logic '1' of between -5 V and -15 V. At the receiving end a voltage of between +3 V and +15 V represents a '0' and a voltage of between -3 V and -15 V represents a '1'. Voltages between ±3 V are undefined and lie in the transition region.

The maximum cable length was originally defined in RS-232C as 15 metres, however this has been revised in EIA-232-D and EIA/TIA-232-E and is now more correctly specified as a maximum capacitive load of 2500 pF. This equates to around 15 to 20 metres line length depending on cable capacitance.

The maximum slew rate of the signal at the output of the driver is 30 V/µs. This limitation is concerned with the problem of cross talk between conductors in a multiconductor cable. The faster the transition edge the greater the cross talk. This restriction together with the fact that the driver and receiver use a common signal ground and the associated noise introduced by the ground current severely limits the maximum data throughput.

For this reason the EIA-232 standard specifies a maximum data rate of 20 kbps.

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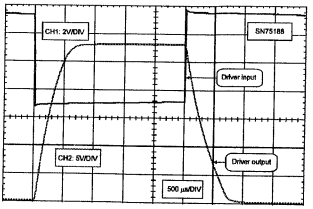
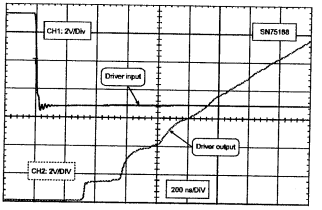
Line Reflections in a V.28 (RS-232) Interface

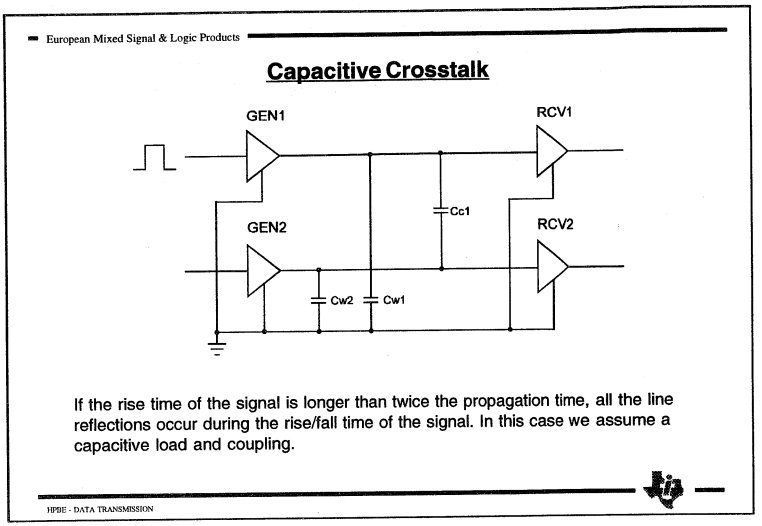




The transmission line theory can be ignored when the rise time of the signal is longer than twice the propagation time.

HPBE - DATA TRANSMISSION

The section 'Basics and Practical Examples of Transmission' comprised the topics termination and line reflections. In the case of the RS-232 interface the receiver input impedance is between 3k - 7 kΩ. A termination resistor is not necessary, because of the slow rise time of the signal. This effect is shown in the figure above, the line reflections occuring during the rise time of the signal.



Capacitive Crosstalk

The capacitive crosstalk in a RS-232 interface can be treated as shown in the figure. If the rise time of the signal is longer than twice the propagation time, all the line reflections occur during the rise/fall time of the signal. In this case it is allowed to assume a capacitive load and coupling. The coupling capacitor is between 0.2 and 1 Cw. This value depends on the type of cable.

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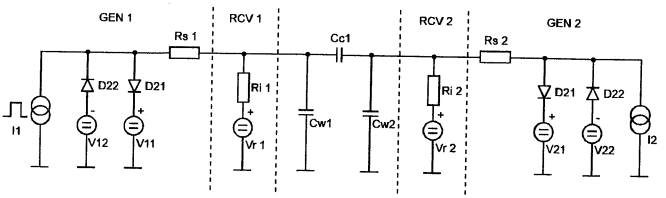
Equivalent Circuit Diagram for Capacitive Crosstalk in a V.28 (RS-232) Interface



The driver may be considered as a voltage limited current source I1 (+/- 10 mA). In conjunction with the line capacity (Cw = 0,5...1pF/cm). This slows rise and fall times, which are dependent on the line length.
(Coupling capacitor Cc approx. 0,2...1 Cw)

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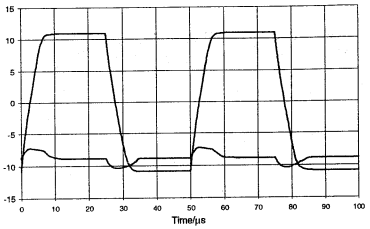
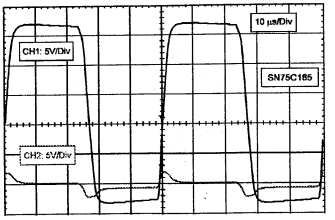
Capacitive Crosstalk in a V.28 (RS232) Interface

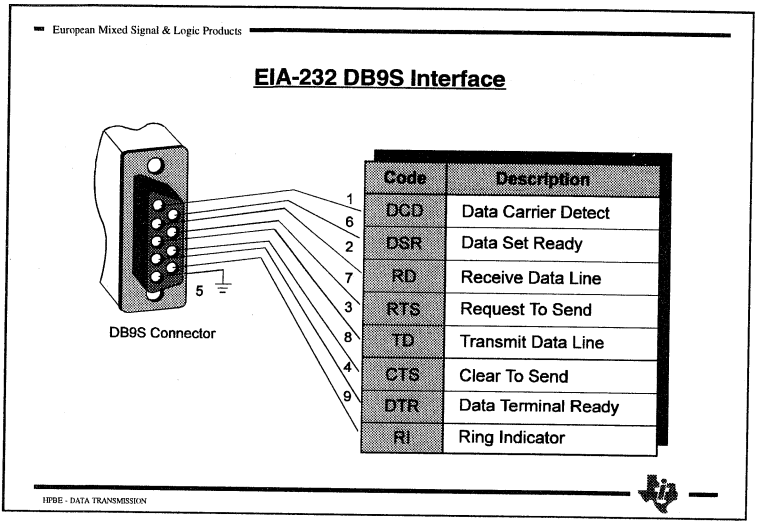


SPICE SIMULATION



MEASUREMENT

The simulation and the measurement show a similar result. The crosstalk doesn't disturb the sytem due to the slew rate limited signals.



The DB9S Connector

Today's notebook and laptop PCs, with their quest for reduced size, no longer use the standard 25-way D-type connector detailed in the standard but have substituted it for a 9-way D-type. This is commonly known as the DB9S connector. Like the 25-way, the DCE equipment connector is a male outer casing with female connection pins, and the DTE is a female outer casing with male connecting pins.

As the interface is now made up of only nine pins the handshaking lines have been reduced accordingly but still are sufficient for most applications. The figure shows the pins assignments for the interconnect cable into the DTE connector. An explanation of the function of each signal is given below:

Data Carrier Detect (DCD) - Received Line Signal Detector

The ON condition on this signal line as sent by the DCE informs the DTE that it is receiving a carrier signal which meets its suitability criteria from the remote DCE. In modems, this circuit is held on as long as it is receiving a signal that can be recognised as a carrier. On half duplex channels, DCD is held off when RTS is in the on condition.

Data Set Ready (DSR)

This is a signal turned on by the DCE to indicate to the DTE that it is connected to the line.

Receive Data Line (RD)

The signals on the RD line are in serial form . When the DCD signal is in the off condition the RD line must be held in the Mark state.

Request to Send (RTS)

This signal is turned on by the DTE to indicate it is now ready to transmit data. The DCE must then prepare to receive data. In half duplex operation, it also inhibits the receive mode. After some delay the DCE will turn the CTS line on to inform the DTE it is ready to receive data. Once communication is over and no more data is transmitted by the DTE, RTS is then turned from on to off by the DTE. After a brief time delay to ensure all data has been received that was transmitted, the DCE turns CTS off.

Transmit Data Line (TD)

The signals on this circuit are transmitted serially from DTE to DCE. When no data is being transmitted the signal line is held in the Mark state. For data to be transmitted, DSR, DTR, RTS and CTS must all be in the on state.

Clear to Send (CTS)

This signal is turned on by the DCE to indicate to the DTE that it is ready to receive data. CTS is turned on in response to simultaneous on condition of the RTS, DSR and DTR signals.

Data terminal Ready (DTR)

This in conjunction with DSR indicate equipment readiness. DTR is turned on by the DTE to indicate to the DCE it is ready to receive or transmit data. DTE must be in the on condition before the DCE can turn on DSR. When DTR is turned off by the DTE, the DCE is removed from the communication channel following the completion of transmission.

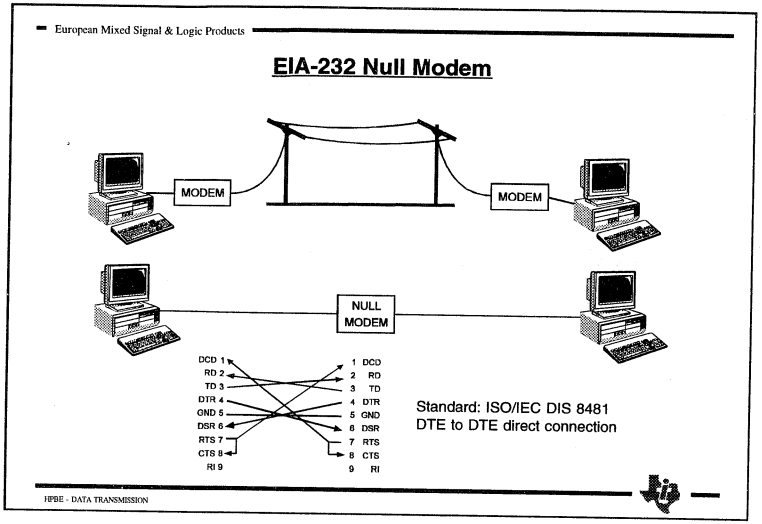
Ring Indicator (RI)

The ring indicator is turned on by the DCE while ringing is being received and is a term left over from the use of the standard in telephone line modem applications. Primarily used in auto-answer systems.

Signal Ground (pin 5)

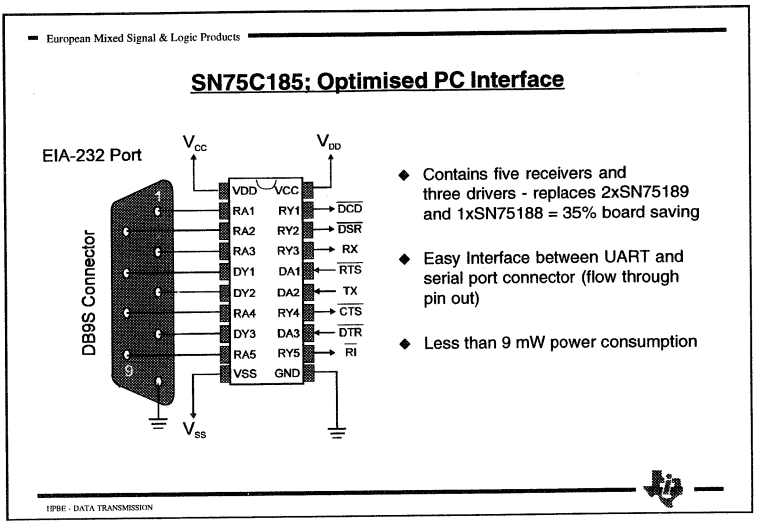
This is the ground which provides the common ground reference for all the interchange circuits and is separate from the protective ground. The protective ground is electrically bonded to the equipment frame and is usually directly connected to the external ground. Any static discharges are then routed directly to ground without affecting the signal lines.

While all these pins are assigned, once again not all equipment uses every pin. Consider the mouse which can use as few as 4 lines, Signal ground, RI, TD and RD. Most equipment does however utilise a minimum of RTS, DTR, TD, RD, CTS and DSR.



EIA-232 Null Modem

The majority of equipment uses the Data Terminal Equipment (DTE) interface and makes use of the null modem as a means of communication between DTEs, without intermediate Data Circuit-terminating Equipment (DCE). The null modem makes use of feeding back the RTS signal to the CTS line on each interface. The figure details the connections for implementing a full null modem for the DB9S connector.

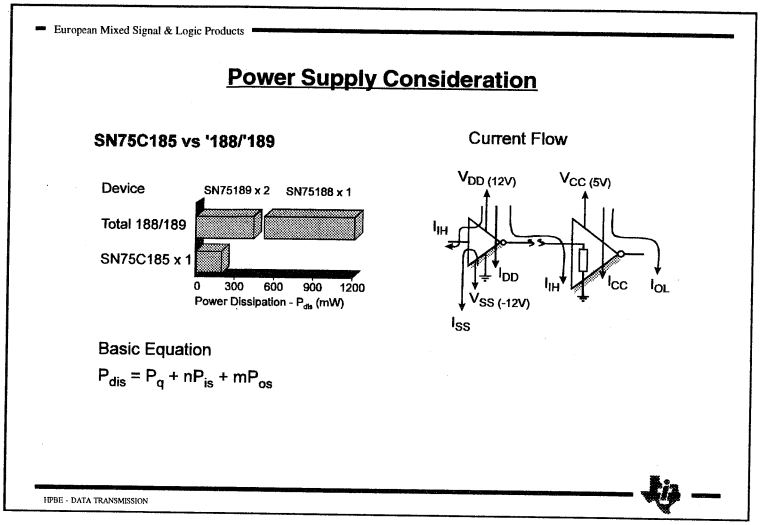


SN75C185: Optimised PC Interface

The DB9S DTE interface consists of 3 transmit lines and 5 receive lines. This is an awkward combination for the standard EIA-232 IC configurations in use today. Consider the ubiquitous SN75188 and SN75189 quad drivers and receivers. To implement this interface would require 3 ICs, one '188 and two '189s. Equal combinations of drivers such as the triple driver/receiver of the SN75C1406 still requires two chips to implement the interface.

For this reason TI has developed the SN75C185. By providing the exact combinations of driving and receiving elements, along with the necessary passive components, a highly optimised solution can be provided – the SN75C185 is just that. The SN75C185 integrates three drivers and five receivers and includes the necessary capacitors for driver slew-rate limit (30 V/µs) and receiver filter implementation, all in a single 20-pin package

The designer's dilemma is eased further by the use of a flow-through pin out architecture. By aligning one side of the SN75C185 with the pins of the DB9S connector and the other to industry standard ACEs or UARTs, printed circuit board (PCB) layout can be greatly simplified.



Low Power with the SN75C185

In common with all of Texas Instruments BiMOS products, these devices combine the benefits of Bipolar's drive capability and robustness along with the low-power consumption of CMOS. This power saving, when compared to the alternatives is calculated in the following pages.

Available in either a single 20-pin, wide-bodied SO pack or DIP pack, the SN75C185 offers designers greater than 25% saving in board space, compared to alternate solutions.

Interface Power Consumption Calculations

Before the availability of the SN75C185 common implementations of EIA-232 require one quad-driver package and two quad-receiver packages; in the driver chip, one device is redundant while in the receiver chips, three devices are redundant. These devices would, however, still be taking their quiescent current and hence wasting power. In order to provide the interface signals, three integrated circuits were required while only two-thirds of the capability was being used. The calculations below demonstrate this difference.

When comparing the 'C185 solution to that provided by the SN75188 and SN75189 devices, the power saving is enormous.

Both implementations require three supply voltages; a 5 V and ±12 V supplies. The power dissipated, P_{dis}, within each device is the quiescent power of the device, P_q, plus the power dissipated in the input stage, P_{is}, and the power dissipated in the output stage, P_{os}, (when it is driving the line).

Hence,

$$P_{dis} = P_q + nP_{is} + mP_{os}$$

Where n is the number of active input stages and m is the number of active output stages.

SN75188/SN75189 Combination

Using an SN75188 for the driver, the quiescent power consumption would be 576 mW. In addition to this the power dissipated in the input stage, Pisd:-

$$P_{isd} = V_{CC} \times I_{IL}$$
$$= 12 \times 1.6 \text{ mW}$$
$$= 19.2 \text{ mW}.$$

This is multiplied by four to take into account all four drivers, putting the fourth driver into a defined state so as to reduce any noise problems that could be introduced by leaving the input floating.

The power dissipated in the output stage, P_{osd}, is:

$$Posd = (VCC - VOH) * \frac{VOH}{RL}$$
$$= (12 - 9) * \frac{9}{3} \text{ mW}$$
$$= 9 \text{ mW}.$$

This figure will be multiplied by three to take into account the active three drivers driving the interface line. These sum up to give a total power dissipation of

$$Pdis = 576 + 4 \times 19.2 + 3 \times 9 \text{ mW}$$
$$= 680 \text{ mW}.$$

The junction temperature of a DIP device would have risen by 74°C.

Using the SN75189 receivers, a quiescent power of 130 mW would be dissipated by each package. This would be multiplied by two to take into account both chips.

The power dissipated in the output stage has a similar equation to that of the driver.

$$P_{osr} = V_{OL} \times I_{OL}$$
$$= 0.45 \times 10 \text{ mW}$$
$$= 4.5 \text{ mW}$$

This power dissipated is multiplied by five to take into account the five receivers being used. The input stage can also dissipate some power, but this power is not supplied by this part of the interface system. The power dissipated within the IC will however cause the junction temperature to rise.

$$Pisr = \frac{(VOH)^2}{RL}$$
$$= \frac{9^2}{3} \text{ mW}$$
$$= 27 \text{ mW}$$

This power dissipation is then multiplied by five. The remaining receivers will require tying to a state where they will not be susceptible to noise. Tying them to the 5 V supply increases the power dissipation by a further 8.3 mW per receiver.

Assuming three receivers in one SN75189 are being used and two receivers in the other, the power dissipated for the first receiver is:

$$P_{dis} = 130 + 4 \times 27 + 3 \times 4.5 \text{ mW}$$
$$= 233 \text{ mW}.$$

The power dissipated in the second receiver is:-

$$P_{dis} = 130 + 4 \times 27 + 2 \times 4.5 \text{ mW}$$
$$= 210 \text{ mW}.$$

This raises the temperature of the first and second receiver by 25°C and 23°C, respectively.

The total power dissipated by the SN75188/189 combination is the sum of these three powers, equalling **1.12 W**.

Using the SN75C185

The power dissipation of the SN75C185 can be calculated in a similar manner. The quiescent-power consumption of the SN75C185 is equal to:-

$$\begin{aligned} P_q &= V_{DD} \times I_{DD} + V_{SS} \times I_{SS} + V_{CC} \times I_{CC} \\ &= 12 \times 200 + -12 \times -200 + 5 \times 750 \quad \mu W \\ &= 8.55 \text{ mW} \end{aligned}$$

The power dissipated in the input stage of the driver is:-

$$\begin{aligned} P_{isd} &= V_{DD} \times I_{IL} \\ &= 12 \times 1 \ \mu W \\ &= 12 \ \mu W. \end{aligned}$$

This is multiplied by three to take into account all of the drivers.

The power dissipated in the output stage of the driver, Posd, is:

$$\begin{aligned} Posd &= (V_{CC} - V_{OH}) * \frac{V_{OH}}{R_L} \\ &= (12 - 10) \times \frac{10}{3} \text{ mW} \\ &= 6.67 \text{ mW}. \end{aligned}$$

This is multiplied by three to take into account the three drivers driving the interface line, giving a power dissipation of 20 mW.

The power dissipated in the output stage of the receiver has a similar equation to that of the driver, so:

$$\begin{aligned} P_{osr} &= V_{OL} \times I_{OL} \\ &= 0.4 \times 3.2 \text{ mW} \\ &= 1.28 \text{ mW} \end{aligned}$$

This value is multiplied by five giving a total of 6.4 mW of power dissipated in the receiver's output stages. The input stage will also dissipate some power, but this power will not be supplied by this part of the interface system. The power dissipated within the chip will however cause the junction temperature to rise.

The power dissipated in the input stage, P_{isr}, equals:

$$\begin{aligned} P_{isr} &= \frac{(V_{OH})^2}{R_L} \\ &= \frac{10^2}{3} \text{ mW} \\ &= 33.3 \text{ mW} \end{aligned}$$

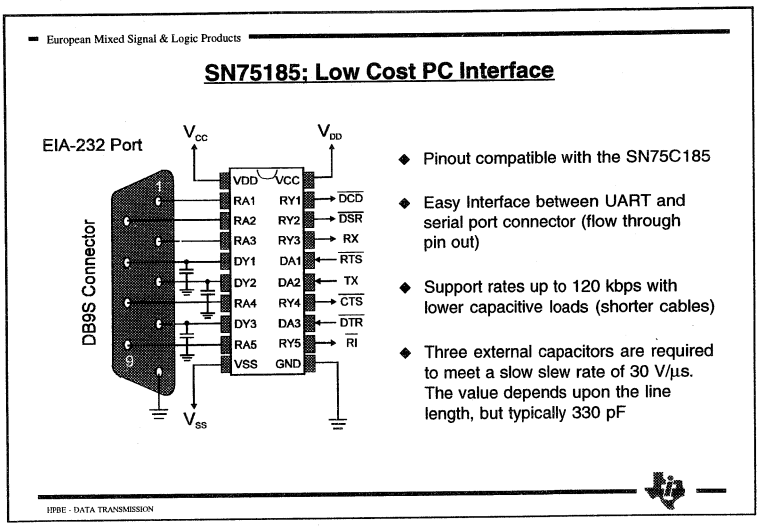
This power dissipation will also require multiplying by five. Giving a total input power dissipation of 167 mW.

Summing all the power contributors the total power dissipation is given by;

$$\begin{aligned} P_{dis} &= P_q + 3P_{isd} + 3P_{osd} + 5P_{isr} + 5P_{osr} \\ &= 8.55 + 3 \times 12 \times 10^{-3} + 3 \times 6.67 + 5 \times 33.3 + 5 \times 1.28 \quad \text{mW} \\ &= 201 \text{ mW}. \end{aligned}$$

The total power dissipated by the SN75C185 is 201 mW

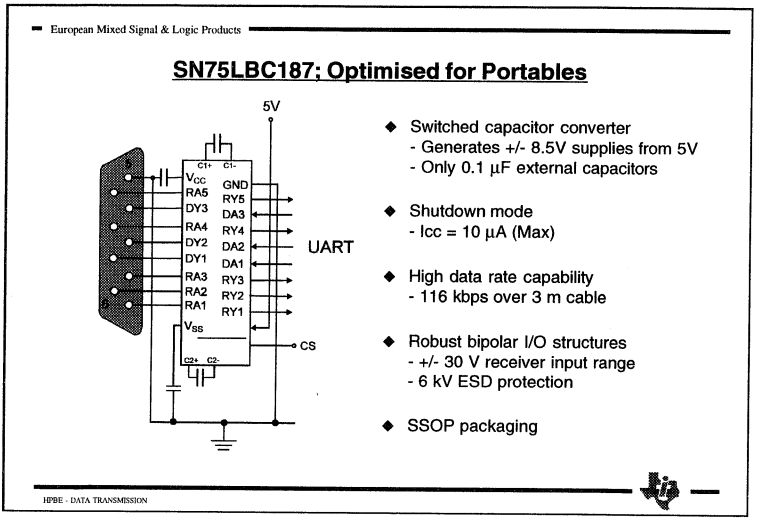
This is represents a tremendous power saving, especially when considering that the line is still being driven. The temperature rise within the SN75C185 would only be 22°C, enabling it to operate more reliably and with higher ambient temperatures.



SN75185: Low Cost PC Interface

The SN75185 combines, like the SN75C185, 3 drivers and 5 receivers. The pinout matches the flow through design of the SN75C185 to decrease the part count, reduce the board space required, and allow easy interconnection of the UART and serial port connector. The bipolar circuits and processing of the SN75185 provides a rugged low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C185.

The switching speeds of the SN75185 are fast enough to support up to 120 kbps with lower capacitive load (shorter cables).



SN75LBC187; Optimised for Portables

The SN75C185 is the ideal choice for computer applications where the bipolar supplies required by EIA-232 are available within a computer system. Most desk top computers generate ±12 volt supplies for powering the internal disk drive. However for portable equipment, e.g. laptops, notebooks, hand held measuring equipment, the EIA-232 interface may be the sole user of a negative supply. The cost of implementing a switch mode supply, using inductive switching regulators, to generate the negative supply can make this option unattractive. Switch mode supplies also have the draw back of increasing the EMI emissions, a factor becoming an increasingly important design constraint. Integrating a switch mode power supply on silicon would reduce the emissions, and has been the dream of semiconductor manufacturers, but thus far no one has yet managed to integrate the inductor.

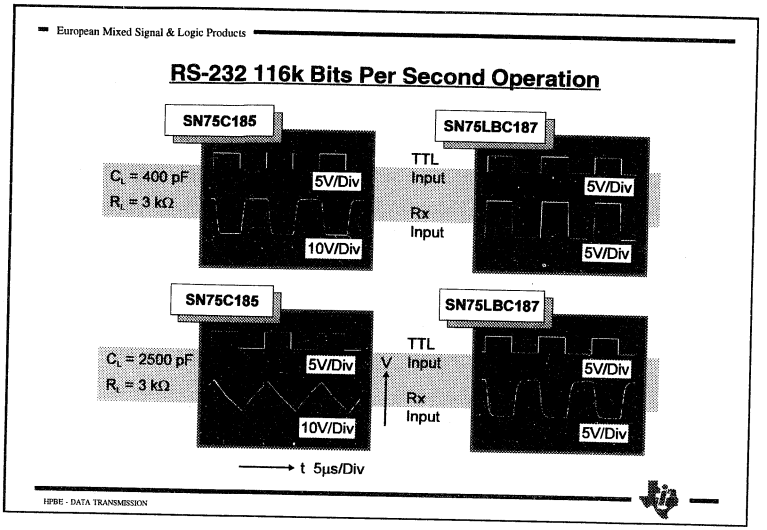
An alternative way, and the basis of modern technology charge pumps, is to make switching regulators using capacitors. In essence they operate by applying charge to a capacitor via an input voltage and then adding, subtracting or inverting the voltage on the positive or negative voltage terminals. This charge is transferred into a holding reservoir capacitor that is then used to supply the output voltages. Furthermore such a scheme can be integrated into silicon. Using a network of capacitors both voltage doublers and invertors can be made.

The SN75LBC187 integrates the charge pump on the same IC as the EIA-232 drivers and receivers. It is fabricated in Texas Instruments' proprietary LinBiCMOS™ technology and contains three independent drivers and 5 independent receivers together with the switched-capacitor voltage converter. The SN75LBC187 provides a single 5 V supply interface between the asynchronous communications element (ACE or UART) and the serial port connector of the data terminal equipment (DTE). This device has been designed to conform to standards EIA/TIA-232-E-1986 and EIA/TIA-562 and CCITT recommendation V.28.

The switched-capacitor voltage converter of the SN75LBC187 uses four small (0.2 μF) external capacitors to generate the positive and negative voltages required by EIA-232 line drivers from a single 5 V logic supply input. Like the SN75C185 the drivers feature output slew-rate limiting to eliminate the need for external filter capacitors. The receivers can accept ±30 V without sustaining damage. Furthermore the 'LBC187 is guaranteed to withstand up to 6KV ESD on any of its pins making it Texas Instruments' most rugged EIA-232 product.

The device also features a reduced power or shutdown mode that virtually eliminates the quiescent power supply when the IC is not active.

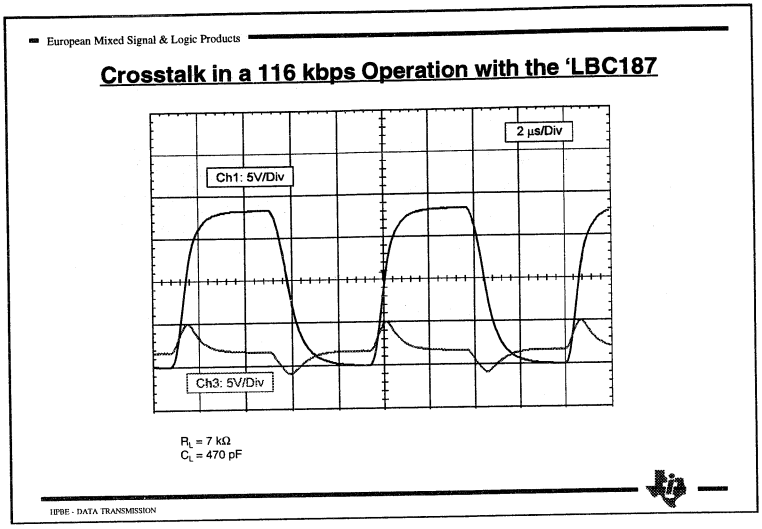
The primary application for the 'LBC187 is for battery operated, portable equipment where power consumption is a key factor. A separate consideration, and one that usually goes hand in hand with these factors, is that of shear physical size. With the 'LBC187, TI has used the latest SSOP packaging to reduce board area to an absolute minimum. The new SSOP package reduces board space to 43% of the standard 28-pin SOIC package Couple this with the small 0.2 μF and you have the ideal single supply solution for space restricted applications.



SN75LBC187; 116 kbps operation

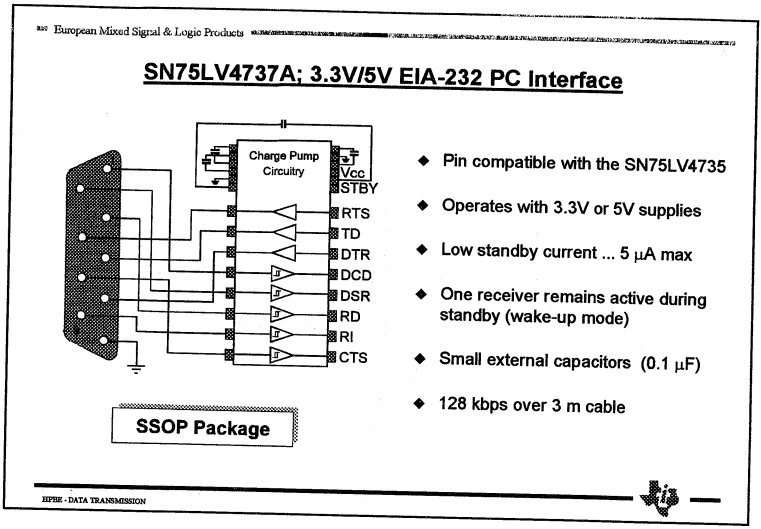
As discussed earlier, the limitation on data rate is one of short circuit output current and the actual load capacitance. With the 'LBC187 the driver short circuit current, IOS, is higher than say the SN75C185 and is therefore able to drive longer line lengths at higher data rates. The figure illustrates this. The 400 pF load in the top half of the figure represents a cable approximately 3 metres long. As the 'scope traces show, the 'C185 produces a perfectly acceptable output trace at 116 kbps. Similarly with the 'LBC187 trace.

If the line length is now upped to 20 metres or 2500 pF load, we can see how the short circuit current limit now limits the slew rate. With the 'LBC187 the trace is still acceptable and will provide reliable data transmission. With the 'C185, the data will still be transmitted but the probability of error is now increased. Most software programs that operate 116 kbps, e.g. Laplink* (Laplink is a trademark of Travelling Software Inc.) provide the interconnect cable as part of the system. In most cases this cable is less than 3 metres in line length so either the 'C185 or 'LBC187 would be able to transmit data reliably. It is interesting to note that both devices would meet EIA-232-D if the rise time to unit interval relationship was extrapolated, however both would fail EIA-232-E. Of course conformance to EIA-232 is not relevant above 20 kbps.



Crosstalk in a 116 kbps Operation

Due to the fact that the output current of the SN75LBC187 is higher, it is important to ensure that the crosstalk of the transmission system is low. The figure illustrates the crosstalk with the SN75LBC187 in a 116 kbps operation. The crosstalk is similar to the investigation with the SN75C185 in a 20 kbps operation.



The SN75LV4737A consists of three drivers and five line receivers, and charge pump circuitry. This combination matches, like the SN75C185 and SN75185, the typical serial port. The charge pump and five small external capacitors allow operation from a single 3.3-V supply and four capacitors for operation from 5-V supply.

The device has flexible control pins for power management when the serial port is active. A common disable for all of the drivers and receivers is provided with the acive-high STBY input. The active-low $\overline{EN}$ input is an enable for one receiver to implement a wake-up feature for the serial port. All the logic inputs can accept signals from controllers operating from a 5-V supply even though the SN75LV4737A is operating from 3.3V.

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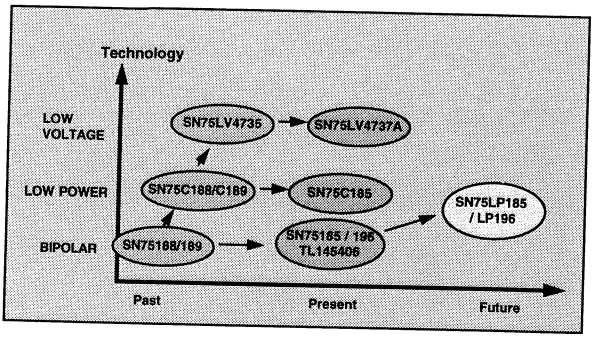
TEXAS INSTRUMENTS DATA TRANSMISSION PRODUCTS
RS232 SELECTION GUIDE

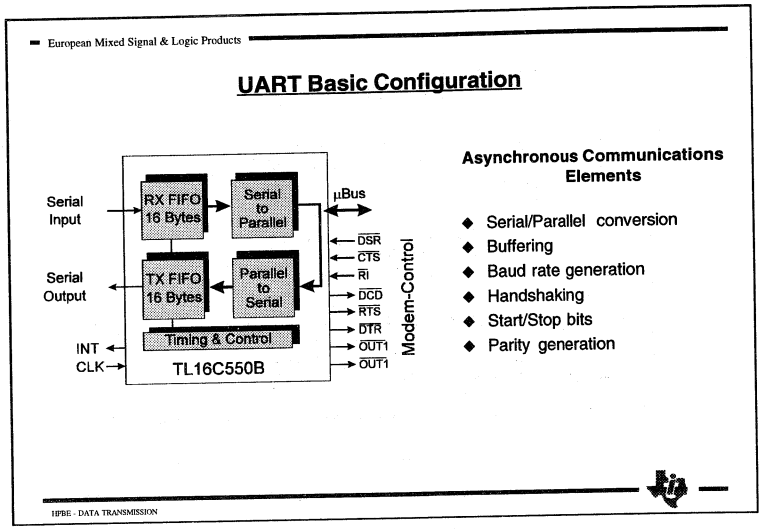
SUPPLIES	SUPPLY(V)	PART #	# DRVRS	# RCVRS	PKGS /#PINS	PRIMARY APPLICATION			
						BATTERY POWERED	NON-BATTERY	PERIPHERAL	COMMENT
SINGLE	3.3V *	SN75LV4735	3	5	DB/28	√			Low Voltage
	3.3 OR 5V *	SN75LV4737A	3	5	DB/28	√			Low Voltage
	5V *	SN75LBC187	3	5	DB/28	√	√	√	
	*	SN75LBC241	4	5	DW/28	√	√	√	
	*	MAX232	2	2	N/16,D/16	√	√	√	
		SN75189/A	0	4	N/14,D/14		√	√	
		SN75C189/A	0	4	N/14,D/14		√	√	Low-power
	5V or +12V	SN75154	0	4	N/16,D/16		√	√	
	± 12V	SN75C188	4	0	N/14,D/14		√	√	Low-power
		SN75C198	4	0	N/14,D/14		√	√	w/ shutdown
		SN75150	2	0	P/8,D/8		√	√	
		SN75155	1	1	P/8,D/8		√	√	
MULTIPLE	5V & ± 12V	SN75C185	3	5	N/20,DW/20		√	√	Low-power
		SN75C1154	4	4	N20,DW20		√	√	Low-power
		SN75C1406	3	3	N/16,D,DW/16		√	√	Low-power
		SN75185	3	5	N/20,DW/20		√	√	
		TL145406	3	3	N/16,DW/16		√	√	
		SN75196	5	3	N/20,DW/20			√	

LOW POWER CHARGE PUMP RS-232 DEVICES

HPBE - DATA TRANSMISSION

RS-232 Roadmap

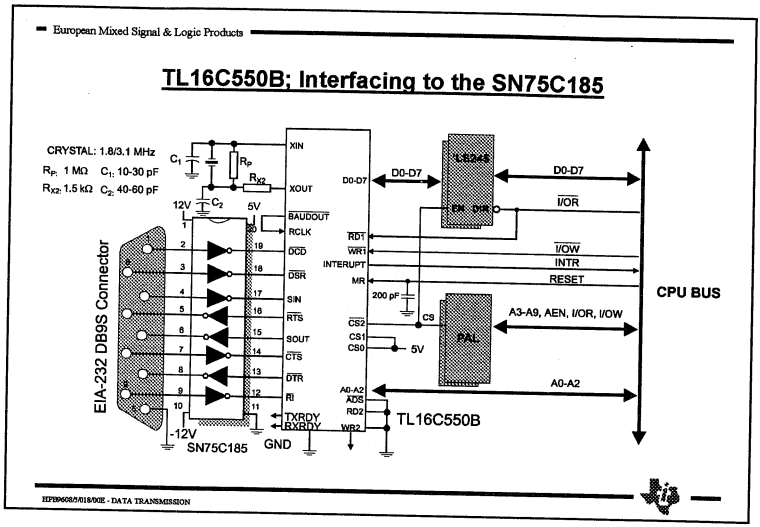




ACEs (UARTs) from Texas Instruments

Most RS-232 systems use dedicated communication controllers. Termed ACEs (Asynchronous Communication Elements) or UARTs (Universal Asynchronous Receiver Transmitter), these devices are responsible for controlling the exchange of information over the RS-232 interface.

The ACE is a dedicated asynchronous communications controller designed to off-load most of the communication activities from the CPU, thus freeing the CPU for other activities. It has the ability to add or delete start and stop bits and provide odd/even parity code generation and detection. Today's components have on board 16-byte or 64-byte receiver- and transmitter FIFO's.



Interfacing Between the TL16C550B and the SN75C185

The circuit shown demonstrates how simple it is to implement in hardware an asynchronous serial interface with the SN75C185 driver/receiver and the communications controller TL16C550B.

When interfacing between the TL16C550B ACE and the Intel CPU bus, little glue logic is required. An 'LS245 Octal bus transceiver is used to provide drive current to an 'off-card' CPU, and programmable array logic (PAL) is used to decode address lines and generate a chip select signal.

Below we discuss the key interface lines.

Xin/Xout:

External clock. Connects the ACE to the main timing reference (clock or crystal).

$\overline{\text{baudout}}$, RCLK:

The transmitter reference clock is available externally via the baudout pin. In this application bpsout is fed into the receiver clock to provide a timing reference for the receiver circuitry. Clock rate is established by the reference oscillator clock frequency (xin) and divided by a driver specified by the bps generator divisor latches.

$\overline{\text{TXRDY}}$:

Transmitter Ready Output. This pin is used during DMA signalling.

$\overline{\text{RXRDY}}$:

Receiver Ready Output. This pin is also used during DMA signalling.

D0 to D7:

Databus. Eight 3-state data lines provide the bi-directional path for data, control, and status information between the ACE and CPU bus.

$\overline{RD1}$, RD2:

Read inputs. When either input is active (high or low respectively) during ACE selection, the CPU is allowed to read status information from the selected ACE register. Since only one of these inputs is required for the transfer of data during the read operation, RD2 is tied to its inactive state, i.e., low.

$\overline{DCD}$, $\overline{DSR}$, SIN, $\overline{RTS}$, SOUT, $\overline{CTS}$, $\overline{DTR}$, $\overline{RI}$:

These signals are the EIA-232 compatible modem control lines. Devices such as the SN75C185 are employed to convert the TTL/CMOS level signals from the ACE to EIA-232 compatible bipolar voltages of between ±5 V to ±15 V. The signal can then be transmitted over distances of up to 15 m.

The advantages of the SN75C185 can be clearly seen by the simplicity of the interface connections. For example, driving/receiving combinations precisely match the interface requirement, plus the pin-out is aligned directly to the DB9S connector.

$\overline{WR1}$, WR2:

Write inputs. A logic applied to $\overline{WRI}$, during ACE selection allows the CPU to write either control words or data into a selected ACE registers. WR2 is tied in active, i.e.: logic low.

INTERRUPT:

When active (high) the interrupt pin informs the CPU that the ACE has an interrupt to be serviced. This interrupt could occur for one of four reasons;

* Receiver error
* Received data available or time-out (FIFO mode only)
* Transmitter holding register empty
* Enable modem status interrupt

The interrupt is reset (deactivated) either when the interrupt has been serviced or by a master reset (MR).

MR:

Master reset. When active (high), MR clears most ACE registers and sets the states of various outputs (i.e. interrupt).

CS0, CS1, $\overline{CS2}$:

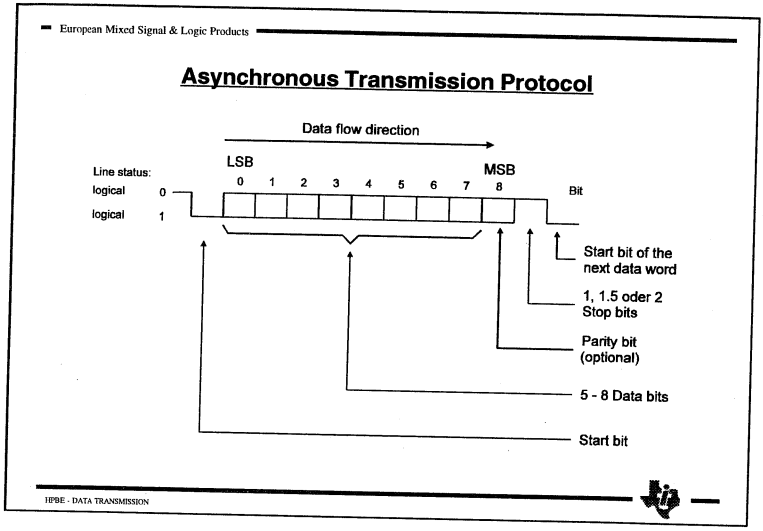
Chip Select. An active low on the $\overline{CS2}$ pin selects the ACE. CS0 and CS1 must be tied active (high) to ensure proper functioning of the $\overline{CS2}$ chip select. A logic high on $\overline{CS2}$ will de-select the ACE.

A0 to A2:

Register Select. These three inputs are used during read or write operations to select the appropriate ACE registers. For example, providing the correct write/read operation had taken place at logic 0 at A2, A1, and A0 would cause the receiver buffer (read) or the transmitter buffer to write.

$\overline{ADS}$:

Address strobe. An active low on ADS, the register select signals (A0 to A2) and chip-select signal ($\overline{CS2}$) drive the internal logic directly.



Asynchronous Transmission Protocol

The asynchronous transmission protocol works in the following way. The transmission starts with the turn of the start bit from high to low level. After the start bit, the transmission of 5-8 data bits follows. An optional parity bit after every character checks the parity of the transmitted character for error detection. The transmission ends with the stop bits. The protocol allows 1, 1.5, and 2 stop bits. After the transmission is completed, the line remains at high level until the start bit turns again to low level.

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Asynchronous Transmission Protocol

Advantages:

- Simple protocol
- Asynchronous, thus no clock signal
- Low cost control circuit (UART)
- Used universally/suitable for a wide range of applications

Disadvantages:

- Low data rate
- Information contains a DC component, thus it is impossible to use an inductive coupling

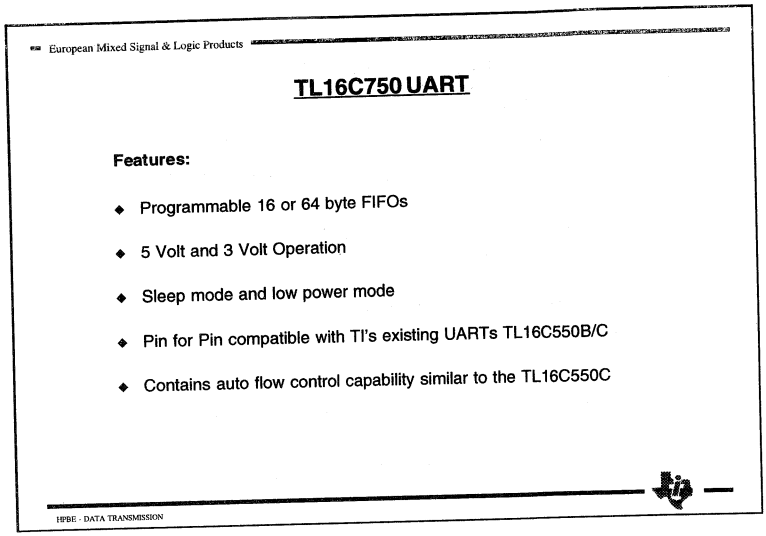
European Mixed Signal & Logic Products

UART Selection Guide

- **TL16C450/451/452**
- **TL16C550B/C** : 16-Byte FIFO/Auto flow control
- **TL16C552A** : Dual 'C550B UART incl. line printer port
- **TL16C554** : Quad 'C550 UART
- **TL16PC564A** : PCMCIA - UART
- **TL16C750** : 'C550 with 64-Byte FIFO and 3.3V/5V capability
- **TL16PNP550A** : Plug-and-Play UART & PnP controller
- **TL16PNP100A/200** : Stand-Alone Plug-and-Play controller
- **TL16PIR552** : incl. 2 IrDA encoder/decoder and IEEE1284 port
- **TIR1000** : Stand-Alone IrDA encoder and decoder
- **TIR2000 *** : 4-Mbps IrDA controller with 64 byte FIFO UART

* Production release planned

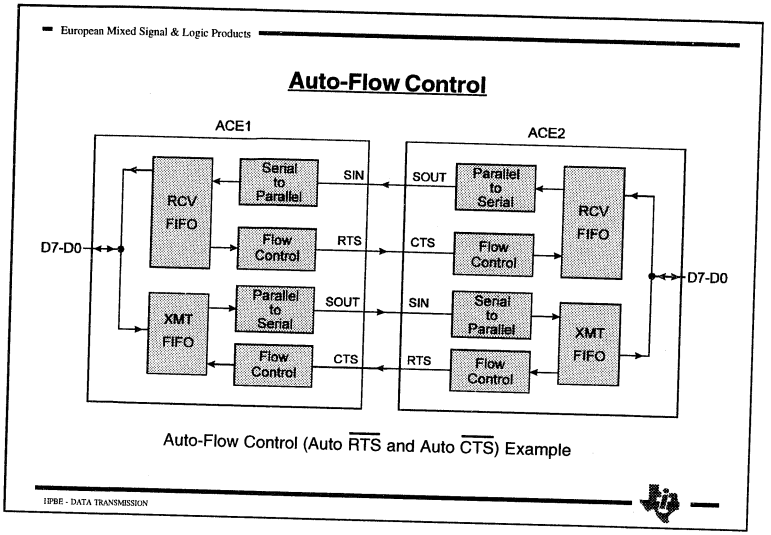
HPBE - DATA TRANSMISSION



TL16C750

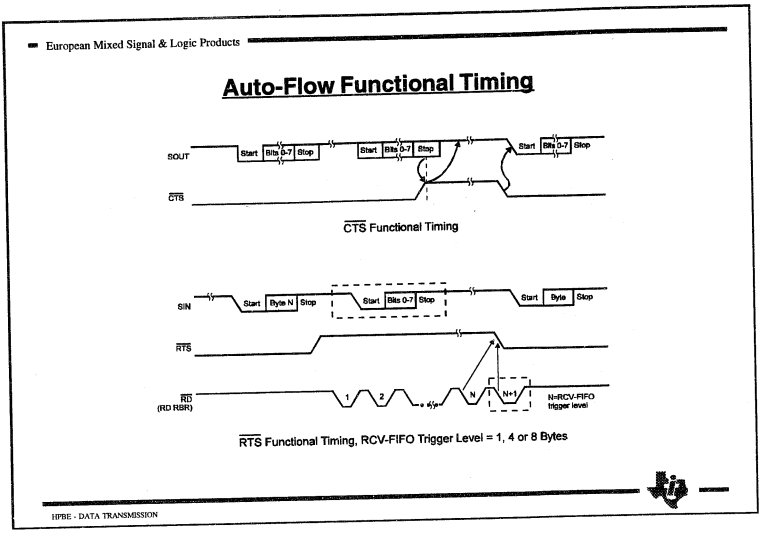
The TL16C750 and the TL16C550 are functional upgrades of the TL16C450. Functionally equivalent to the TL16C450 on power up (character mode or TL16C450 mode), the TL16C750 and the TL16C550, can be placed in an alternate mode (FIFO mode). This relieves the CPU of excessive software overhead by buffering received and transmitted characters. The receiver and transmitter FIFO's store up to 64 bytes including three additional bits of error status per byte for the receiver FIFO. The user can choose between a 16-byte FIFO mode or an extended 64-byte FIFO mode. In the FIFO mode, there is a selectable auto-flow control feature that can significantly reduce software overload and increase system efficiency by automatically controlling serial data flow via the $\overline{RTS}$ output and the $\overline{CTS}$ input signals.

Difference between the TL16C750 and the TL16C550C		
	TL16C750	TL16C550C
FIFO depth	16-or 64-byte	16-byte
Supply Voltage	5-V and 3-V	5-V
Sleep/Low-Power Mode	Yes	No



Auto-Flow Control

Auto-flow control is comprised of auto-$\overline{\text{CTS}}$ and auto-$\overline{\text{RTS}}$. With auto-$\overline{\text{CTS}}$, $\overline{\text{CTS}}$ must be active before the transmit FIFO can emit data. With auto-$\overline{\text{RTS}}$, $\overline{\text{RTS}}$ becomes active when the receiver is empty or the threshold has not been reached. If $\overline{\text{RTS}}$ is connected to $\overline{\text{CTS}}$, data transmission does not occur unless the receive FIFO has empty space. Thus, overrun errors are eliminated if ACE1 and ACE2 are TL16C750s with enabled auto-flow control. If not, overrun errors occur if the transmit data rate exceeds the receive FIFO-read-latency.

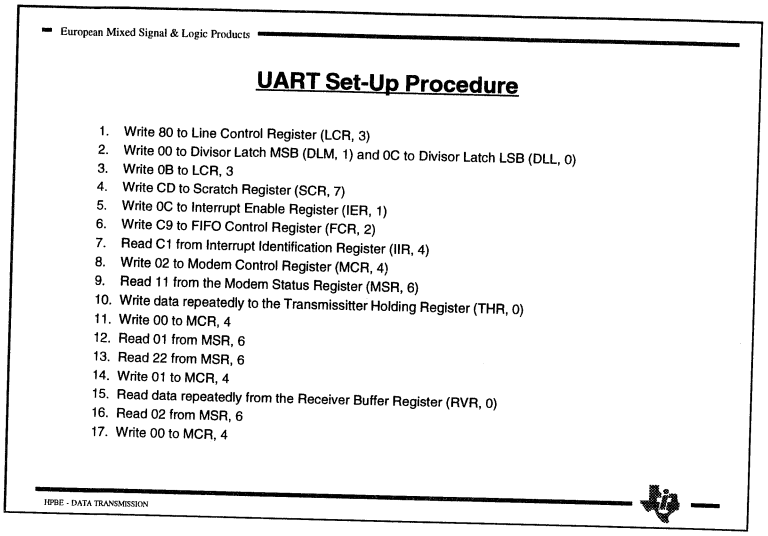


Auto-$\overline{\text{RTS}}$

Auto-$\overline{\text{RTS}}$ data-flow control originates in the receiver timing and control block and is linked to the programmed RCV-FIFO trigger level. When the RCV-FIFO level reaches a trigger level of 1, 4, 8, or 14 in 16-bye mode or 1, 16, 32, or 56 in 64-bye mode, $\overline{\text{RTS}}$ is deasserted. The sending ACE may send an additional byte after the trigger level is reached (assuming the sending ACE has another byte to send) because it may not recognize the deassertion of $\overline{\text{RTS}}$ until after it has begun sending the additional byte. $\overline{\text{RTS}}$ is automatically reasserted once the RCV FIFO is emptied by reading the receiver buffer register (RBR). The reassertion signals the sending ACE to continue transmitting data.

Auto-$\overline{\text{CTS}}$

The transmitter circuitry checks $\overline{\text{CTS}}$ before sending the next data byte. If $\overline{\text{CTS}}$ is active, the transmitter sends the next byte. To stop the transmitter from sending the following byte, $\overline{\text{CTS}}$ must be released before the middle of the last bit that is currently being sent. The auto-$\overline{\text{CTS}}$ function reduces interrupts to the host system. When flow control is enabled, the $\overline{\text{CTS}}$ state changes and does not trigger host interrupts because the device automatically controls its own transmitter. Without auto-$\overline{\text{CTS}}$, the transmitter sends any data present in the transmit FIFO and a receiver overrun can result.



Typical UART Set-Up Procedure

This example demonstrates the transfer between to nodes using a RTS/CTS protocol. Both devices will use fifo mode of operation with the receive fifo threshold set at 14 bytes, and mode 1, dma transfer will be used. The data words will be eight bits wide and transmission will use odd parity with one stop bit. The transmitter and receiver will use the same clock frequency, i.e., the BAUDOUT output will be connected to the RCLK input.

1. Write 80 to Line Control Register (LCR, 3)

This sets the Divisor Latch Access Bit (DLAB) which allows access to the two divisor latch bytes which share addresses with the Receive/Transmit Buffer abd the Interrupt Enable Register (IER).

2. Write 00 to Divisor Latch MSB (DLM, 1) and 0C to Divisor Latch LSB (DLL, 0)

This sets divisor to decimal 12 which programs a baud rate of 9600 for a 1.84MHz clock, 1.8432M/16 = 115.2k/12=9600. The divide by 16 represents the 16x clock rate ration between the data and the clock.

3. Write 0B to LCR, 3

This first turns off the DLAB bit so acceddes to addresses 0 and 1 will be directed to the Receive/Transmit buffers and IER. It also sets the word length to eight bits (vs 5, 6, 7), number of stop bits to one, enables parity, and selects odd parity.

4. Write CD to Scratch Register (SCR, 7)

This has no effect on the operation of the UART, but is just to illustrate that this register can be used as a one byte memory.

5. Write 0C to Interrupt Enable Register (IER, 1)

This enables the modem status interrupts and the receiver line status interrupts. The modem status int is used to signal changes in CTS to handle the protocol, and the line status int is only provided to handle error cases such as parity or overrun errors. The modem status reints are expected but the line status ints are not. The received data available and transmit buffer empty interrupts have intentionally been disabled because the data will be moved back and forth by externally DMA controller rather that under mP control.

6. Write C9 to FIFO Control Register (FCR, 2)

This sets the receiver trigger level to 14, enables DMA mode 1, and enables the fifos for operation. DMA mode 1 causes the $\overline{\text{TXRDY}}$ signal to be asserted whenever the transmit fifo is less than full, and also causes the $\overline{RXRDY}$ signal to be asserted until the rcv fifo is emptied.

7. Read C1 from Interrupt Identification Register (IIR, 2)

This read is just one sanity check that the device has been programmed correctly and is ready for operation. The C indicates that the fifos have been enabled and the 1 indicates that no interrupts are pending. Also note that at start up $\overline{\text{TXRDY}}$ will be asserted and will be deasserted.

8. Write 02 to Modem Control Register (MCR, 4)

This sets the RTS bit and asserts the $\overline{\text{RTS}}$ output pin. It is used to signal a receiver that the device is ready to transmit some data. Note that the modem control lines, either input or output, do not have any effect on the parallel to serial or serial to parallel data flow. They interact only through µC control.

9. Read 11 from the Modem Status Register (MSR, 6)

This is an indication from the receiver that the $\overline{\text{CTS}}$ has been asserted and that there has been a change in the $\overline{\text{CTS}}$ signal since the last read of the MSR. An interrupt will be generated to the mP which will inform it to wake µP the DMA controller to load data into the trransmit buffer.

10. Write data repeatedly to the Transmitter Holding Register (THR, 0)

This loads the transmit fifo and starts transmission of serial data out on SOUT. The first serial byte will take about 100 ms to transmit, so it is likely that the transmit fifo will fill before the first byte has been sent, which will cause the $\overline{\text{TXRDY}}$ to deassert.

The receiving side may release CTS if it cannot keep up with the data stream. In this case, the uP would have to pause the DMA since the internal logic within the UART does not use the modem control signals to direct the data flow.

11. Write 00 to MCR, 4

This clears the RTS bit and releases the $\overline{\text{RTS}}$ signal, signifying that the transmission is complete. The uP must halt the DMA controller before clearing $\overline{\text{RTS}}$.

12. Read 01 from MSR, 6

This indicates that the receiving side has released its $\overline{CTS}$ in response to the transmitting side dropping $\overline{RTS}$.

13. Read 22 from MSR, 6

This informs the uP that the $\overline{DSR}$ input has been asserted, requesting the receiver to accept data. The DSR delta bit is also set.

14. Write 01 to MCR, 4

This indicates that the receiver is ready to accept data by setting $\overline{DTR}$.The uP must first prime the DMA controller before setting $\overline{DTR}$.

15. Read data repeatedly from the Receiver Buffer Register (RCV, 0)

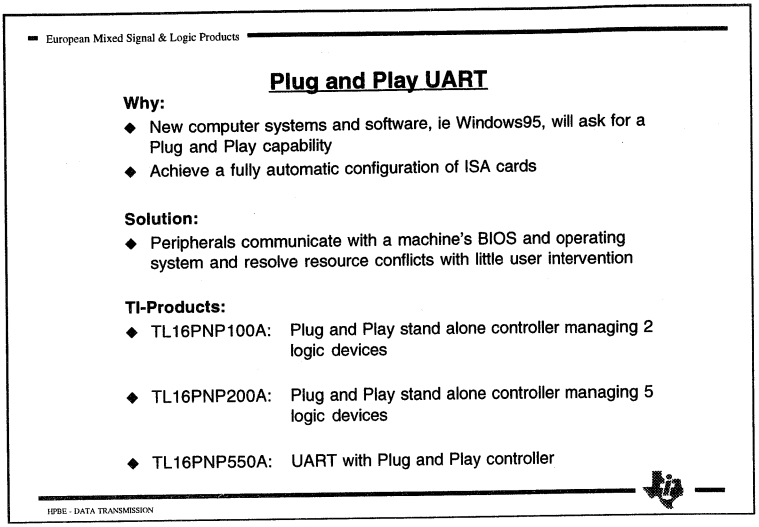
After 14 bytes have been received (or fewer bytes with a timeout), the UART signals the DMA with $\overline{RXRDY}$ to tell it to unload data.

16. Read 02 from MSR, 6

The sending side indicates that it has completed and releases $\overline{DSR}$.

17. Write 00 to MCR, 4

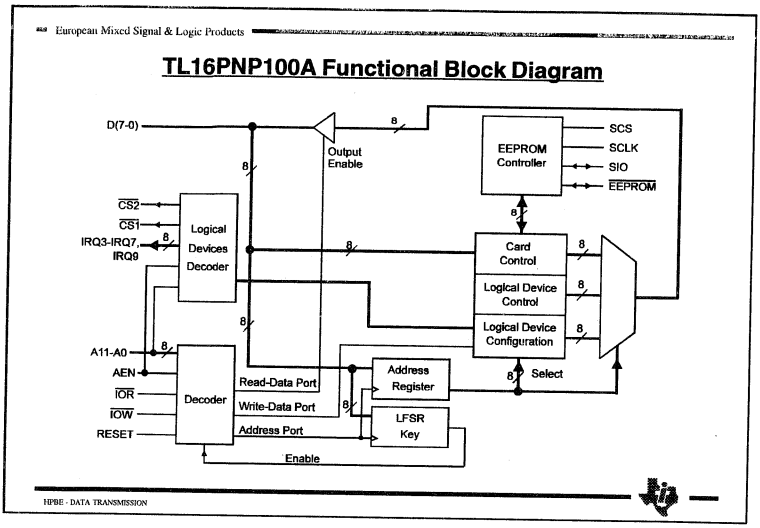
The receiving side clears $\overline{DSR}$ in response to $\overline{DSR}$ being dropped.



Plug and Play

The ISA bus is the most popular expansion standard in the PC industry. The bus architecture requires the allocation of memory and I/O address spaces, DMA channels and interrupt levels among multiple ISA cards. However, the ISA interface has no defined hardware and software mechanism for allocating the resources. As a result, configuration of ISA cards is typically done with 'jumpers' that change the decode maps for memory and I/O space and steer the DMA and interrupt signals to different pins on the bus. Further, system configuration files may need to be updated to reflect these changes. Users typically resolve sharing conflicts by referring to documentation provided by each card manufacturer.

In a system that uses only Plug and Play ISA cards, it will be possible to achieve fully automatic configuration.



TL16PNP100A

The TL16PNP100A responds to the plug and play autoconfiguration process. The process puts all PnP cards in a configuration mode, isolates one PnP card at a time, assigns a card-select number (CSN), and reads the cards's resource-data structure from the EEPROM. After the resource requirements and capabilities are determined for all cards, the process uses the CSN to configure the card by writing to the configuration registers. The TL16PNP100A implements configuration registers only for I/O applications with two logical devices, and no DMA application support is provided. Finally, the process activates the TL16PNP100A card and removes it from configuration mode. After the configuration process, the logic function can then start responding to ISA bus cycles. The controller disables the EEPROM interface after the configuration is complete to allow another on board controller to access to the EEPROM.

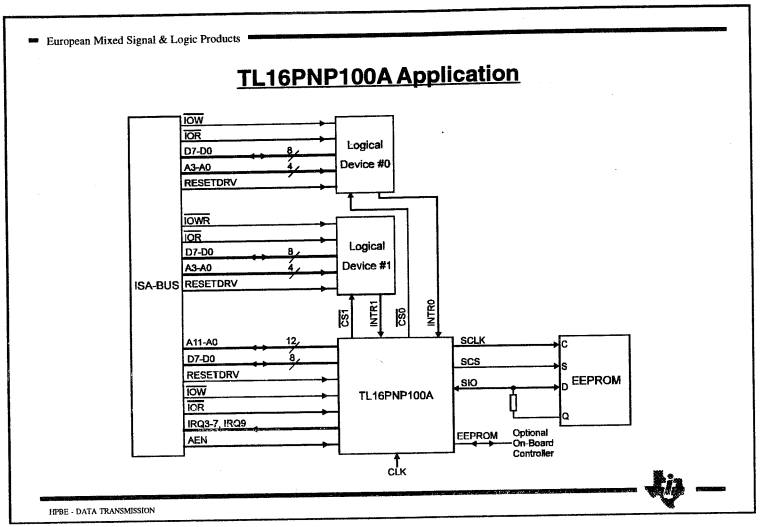
TL16PNP100A Functional Block Diagram

Three 8-bit ports (ADDRESS, WRITE_DATA, READ_DATA) are used by the software to access to configuration space on each Plug and Play ISA card.

The Plug and Play logic is quiescent on power-up and must be enabled by software. This is done by a predefined series of writes to the ADDRESS port. The write sequence is decoded by on card logic (LFSR, linear feedback shift register).

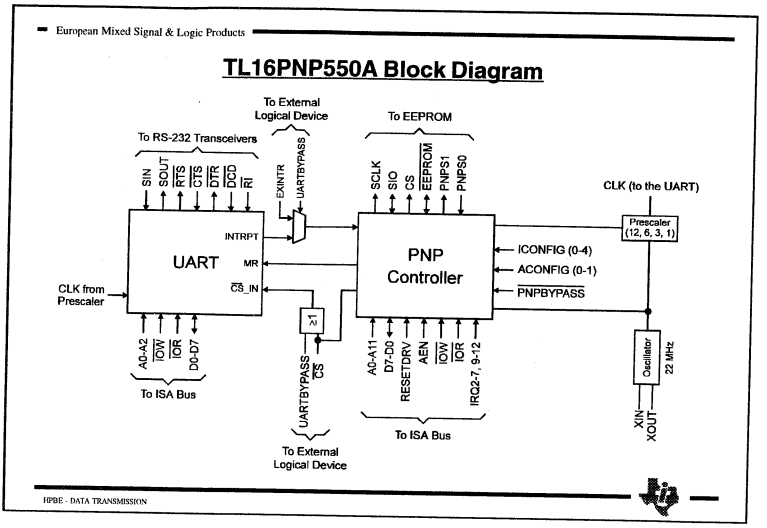
The Plug and Play card standard registers are divided into three parts; card control, logical device control, and logical device configuration. There is exactly one of each card control register on each ISA card. The card control register is used for global functions that control the entire card. The logical device control registers and the logical device configuration registers are repeated for each logical device. The logical device control registers contro device functions, such as enabling the device onto the ISA bus. The logical device configuration registers are used to program the device's ISA bus resource use.

On board is the EEPROM controller that interfaces directly to the EEPROM without any further glue logic.



TL16PNP100A Application

The figure shows a TL16PNP100A application. Two logical devices are controlled by the TL16PNP100A stand-alone Plug and Play controller. An EEPROM is directly connected to the Plug and Play controller where the system resources are stored.

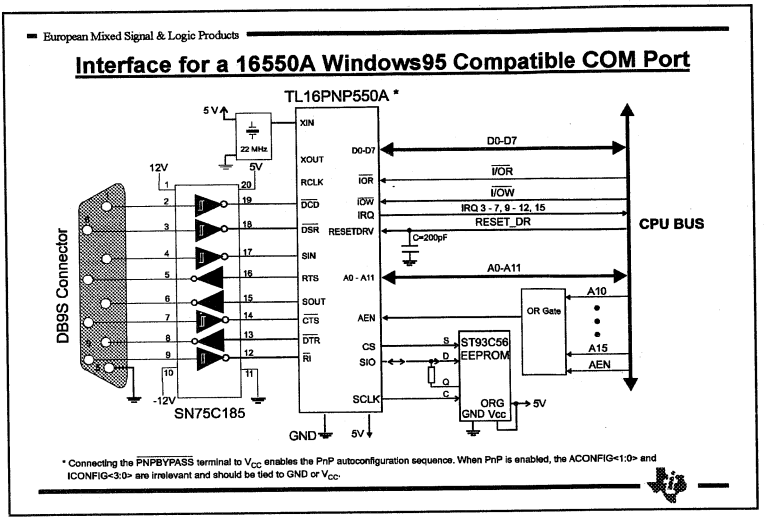


TL16PNP550

The TL16PNP550 responds to the plug and play auto-configuration process. The process puts all PnP cards in a configuration mode, isolates one PnP card at a time, assigns a card select number (CSN), and reads the card resource data structure from the EEPROM. After the resource requirements and capabilities are determined for all cards, the process uses the CSN to configure the card by writing to the configuration registers. The TL16PNP550 only implements configuration registers for I/O applications with one logical device and no DMA support. Finally, the process activates the TL16PNP550 card and removes it from configuration mode. After the configuration process, the ACE starts responding to ISA bus cycles. The device can also be configured to bypass the PnP auto configuration sequence. In this mode the device can also be configured to select the COM port address and IRQ level (the TL16PNP550 provides 10 interrupts). In the UART bypass mode, the UART is disabled and the device is configured to be a stand alone PnP controller that supports one logical device and no DMA support.

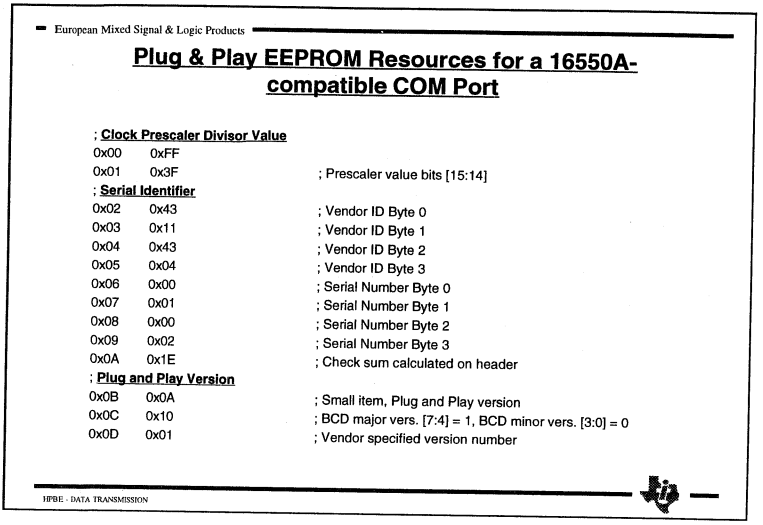
TL16PNP550 Block Diagram

The block diagram of the TL16PNP550 shows that there are two separate blocks for the ACE (UART) and the PnP Controller. This means, the device can be used as separate ACE and PnP controller. That is, the PnP controller provides a chip select signal for an external logical device, or as a PnP UART.



Interface for a 16550A Windows95 Compatible COM Port

The picture above shows an interface for a 16550A Windows95 compatible COM port using the TL16PNP550A. The circuit diagram is similar to a standard RS-232 interface with a TL16C550B UART. The Plug and Play compatible COM port needs a further interface to an EEPROM which stores the resource data. The content of the EEPROM is shown and explained on the following pages.



Plug and Play EEPROM Resources for a 16550A-compatible COM Port

Resource data is used to describe a Plug and Play card to system software. The example shows the EEPROM resources for a 16550A-compatible COM port.

Clock prescaler divisor value

The TL16PNP550 includes a clock prescaler block. The block takes the 22 MHz input clock and divides it by a divisor read from the EEPROM at address zero. After reset, the device reads the EEPROM's content at address zero. The 2 most significant data bits of the word (2 bytes) define the divisor value as follows:

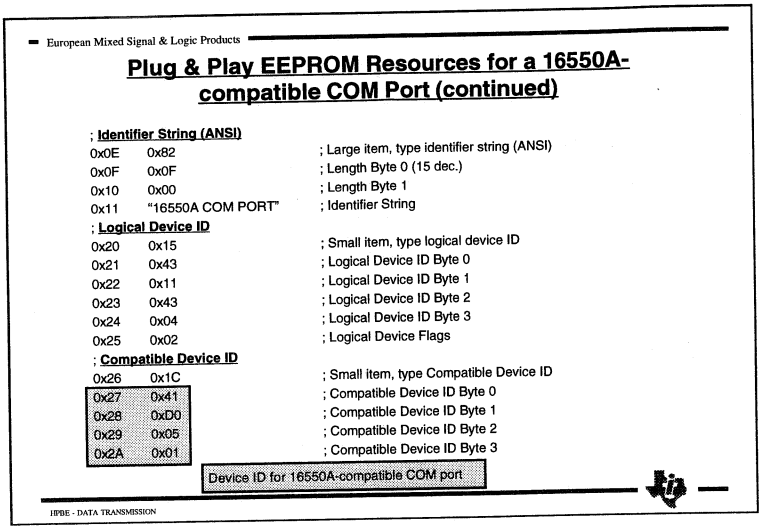
EEPROM Location	
000 (Bits 15 and 14)	Divisor Value
00	12
01	6
10	3
11	1

Serial Identifier

The Serial Identifier consists of the Vendor ID and the Serial Number. The 32-bit Vendor ID is an EISA Product Identifier (ID). The 32-bit serial number is used only in the isolation process for selection of individual Plug and Play ISA cards.

Plug and Play version

The Plug and Play Version Number identifies the version of the Plug and Play specification with which this card is compatible.



Plug and Play EEPROM Resources for a 16550A-compatible COM Port (continued)

Identifier String (ANSI)

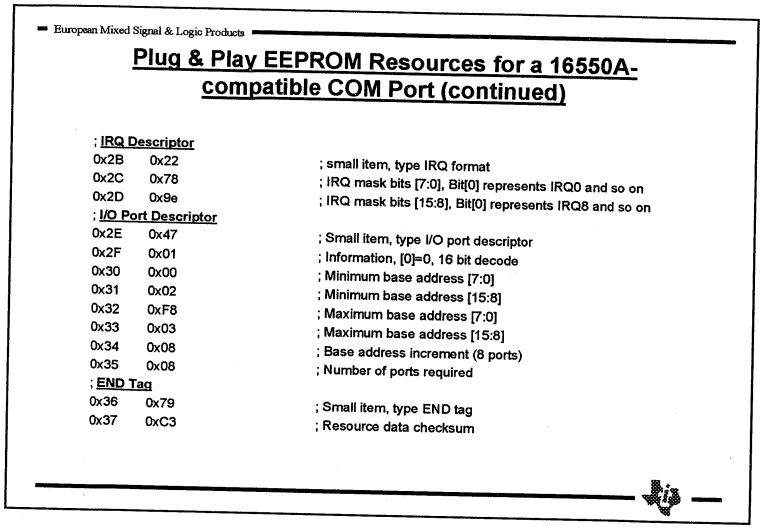
The identifier string is 8-bit ANSI. The length of the string is defined in the structure so the string does not need to be zero terminated. Display software will insure the proper termination gets added to the string. Each card is required to have an identifier string.

Logical Device ID

The Logical Device ID provides a mechanism for uniquely indentifying multiple logical devices embedded in a single physical board.

Compatible Device ID

The Compatible Device ID provides the Ids of other devices with which this device is compatible. The operating system uses this information to load compatible device drivers if necessary. In the example, the Compatible Device ID represents the code for a 16550A-compatible COM port.



Plug and Play EEPROM Resources for a 16550A-compatible COM Port (continued)

IRQ Descriptor

The IRQ data structure indicates that the device uses an interrupt level and supplies a mask with its set indicating the levels implemented in this device. For standard ISA implementation there are 16 possible interrupt levels so a two byte field is used.

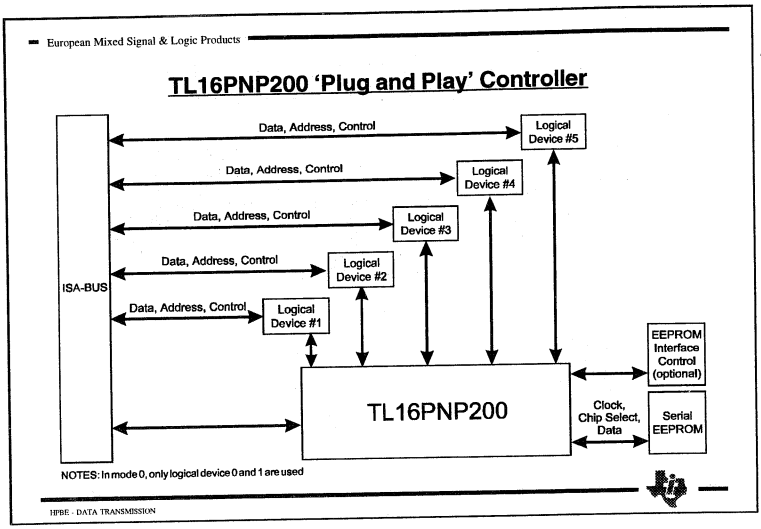
I/O Port Descriptor

There are two types of description for I/O ranges. The first descriptor is a full function descriptor for prammable ISA cards. The second descriptor is a minimal descriptor for ISA cards with fixed I/O requirements that use a 16-bit ISA address decode.

END Tag

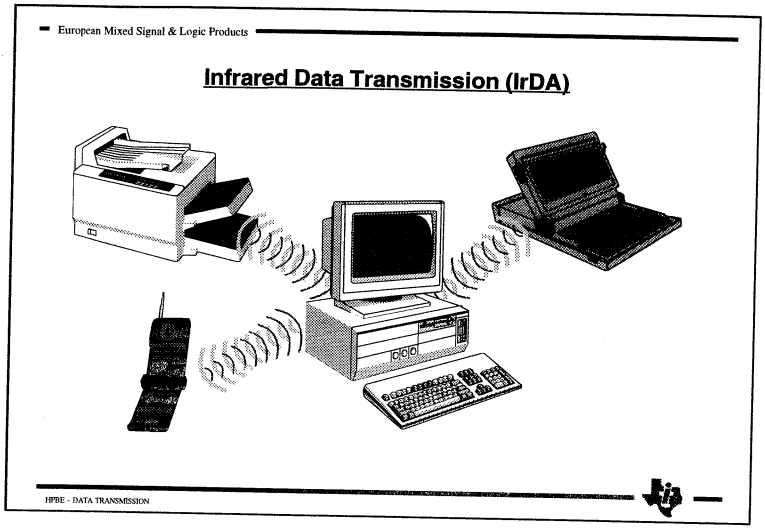
The End tag identifies an end of resource data.

For more detailed information, please refer to the 'Plug and Play ISA Specification', Version 1.0a, May 5, 1994.



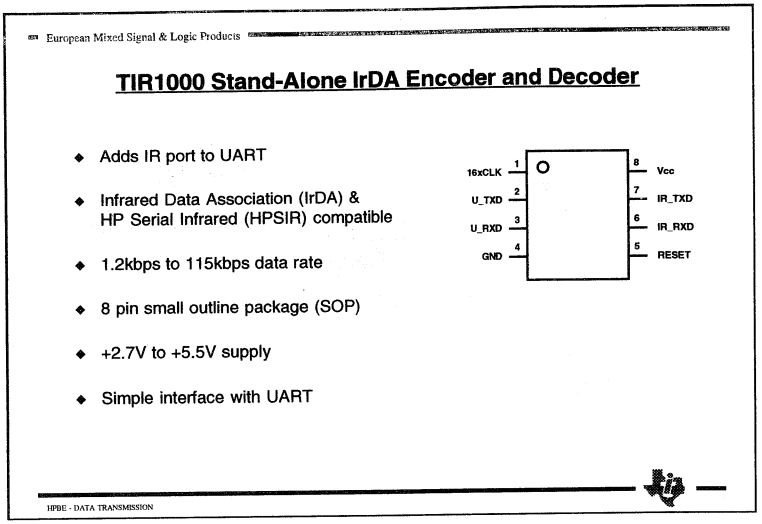
TL16PNP200

The TL16PNP200, which fully satisfies all Windows 95 requirements, is designed to meet the needs of designers of high-end applications such as ISDN, sound and video cards that typically have larger memory and logical device requirements. Like the 'PNP100A, this device is a stand-alone plug-and-play controller with simple memory interface and plug-and-play auto configuration capabilities. In addition, the 'PNP200 can support up to five logical devices in two modes of operation for maximum design flexibility. Mode 0 supports two devices and offers memory, I/O interrupt and direct memory access (DMA) for each of the devices. Mode 1 supports five devices with both I/O and interrupts and supports DMA for two of the logic devices. The 'PNP200 gives designers access to the full range of system resources. It offers a full 16 bits of I/O address in addition to 24 bits of memory address decoding. The device also enables interrupt mapping of 11 interrupt request signals on the ISA bus. In addition, the TL16PNP200 interfaces using 3-pins to an external EEPROM, where resource data, power up defaults and other board specific data can be stored.



Infrared Data Transmission (IrDA)

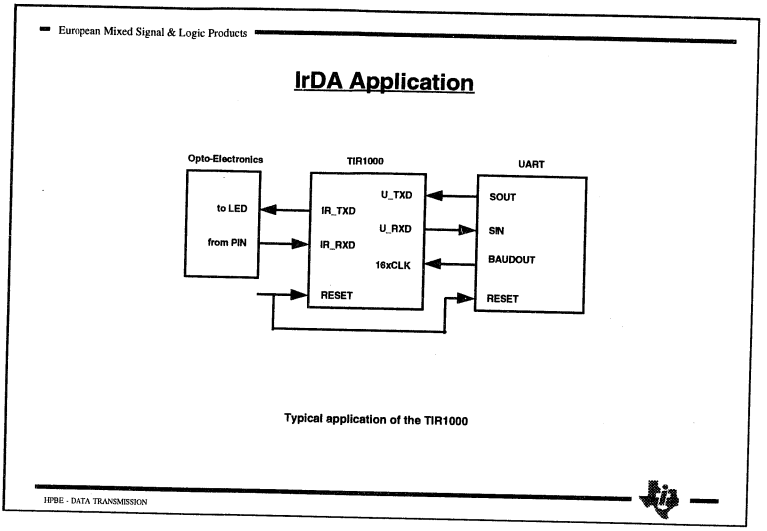
Infrared data transmission has been around for over a decade, but its recent popularity has been fueled by the need for laptop and palmtop computers to make connections and exchange data with the rest of the office network. The arrival of the IrDA (Infrared Data Association) working standard for infrared data links is creating a cheap, easy way for all kinds of devices to exchange information. Despite its moderate speed (115 kbps) and limited range (3-to 6-feet), the IrDA link is quickly gaining popularity because of its simple protocol and inexpensive hardware.



TIR1000 Stand-Alone IrDA Encoder and Decoder

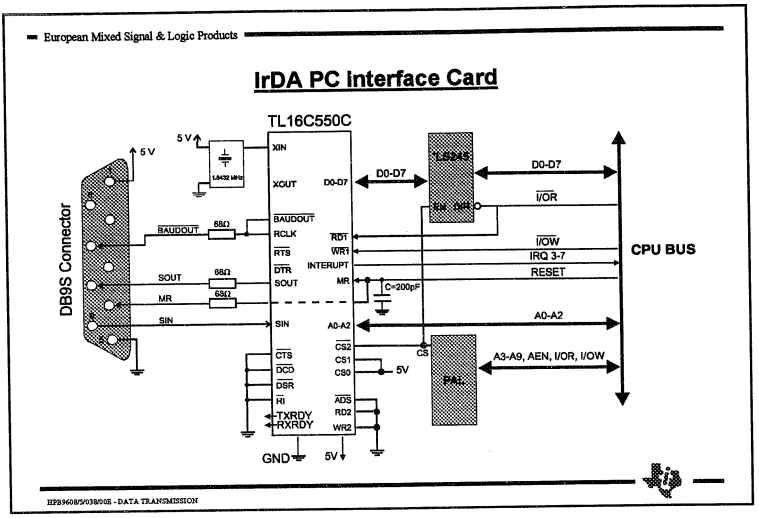
The TIR1000 SIR-Encoder/Decoder is a CMOS device which will encode and decode bit data in conformance with the IrDA specification.

A transceiver device is needed to interface to the PIN and LED. A UART is needed to handle the serial data lines.



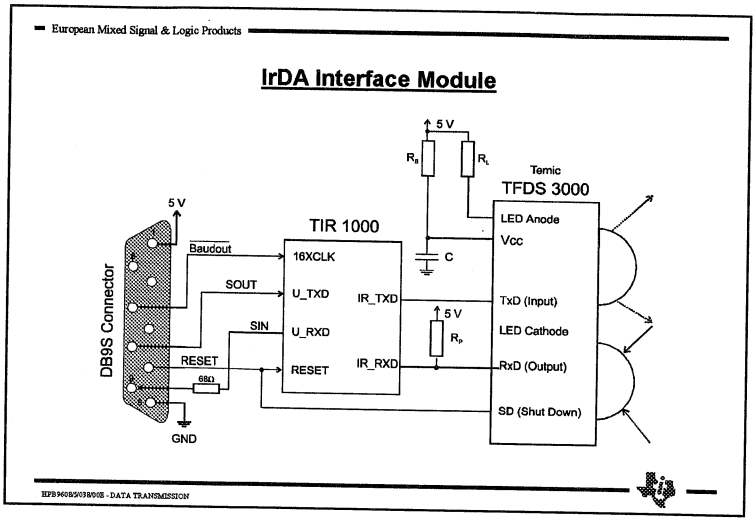
IrDA overview

The Infrared Data Association (IrDA) defined a simple generic protocol for sending and receiving serial infrared data. At a higher level, a serial infrared data 'word' is surrounded by a start bit = 0 and a stop bit = 1. Individual bits are encoded or decoded the same whether they are start , data or stop bits. This part evaluates only single bits. IrDA is specified to run at 115200 bits/s, but can run at a lower rate. The clock used to code or sample the data is 16 times the baud rate, or 1.843 MHz maximum. To code a 1, no pulse is sent or received for 1 bit time or 16 clocks. To code a 0, one pulse is sent or received within 1 bit time or 16 clocks. That pulse must be at least 1.6µs wide, 3 clocks at 1.843 MHz. At lower baud rates the pulse can be 1.6µs wide or as long as 3 clocks. The transmitter output, IR_TXD, is intended to drive a light-emitting diode (LED) circuit to generate an infrared pulse. The LED circuit works on positive pulses. A photo-sensitive diode (PIN) circuit is expected to create the receiver input, IR_RXD. Most, but not all, PIN circuits have inversion, and generate negative pulses from the detected infrared light. Their output is normally high. The TIR1000 can decode either negative or positive pulses on IR_RXD.



IrDA PC Interface Card

The circuit shown demonstrates an IrDA PC interface card which interfaces to an infrared module which is described on the following page. Again, as for the interface between the TL16C550 to the SN75C185, only a little glue logic is required to interface between the TL16C550 and the Intel CPU bus. An '245 bidirectional bus transceiver is used to provide the drive current and a 8-bit comparator with a PAL to decode address lines and generate a chip select signal. It is not necessary to implement a level converter like for an RS232 interface, because we interface the UART directly to the TIR1000 encoder/decoder component which encodes and decodes the bit data in conformance with the IrDA specification. The interface to the IrDA opto module can be performed with a DB9S cable. To avoid line reflections between the PC card and the opto module, three 68 Ω series resistors are connected in series to the output of each driver to match the output impedance of the driver.



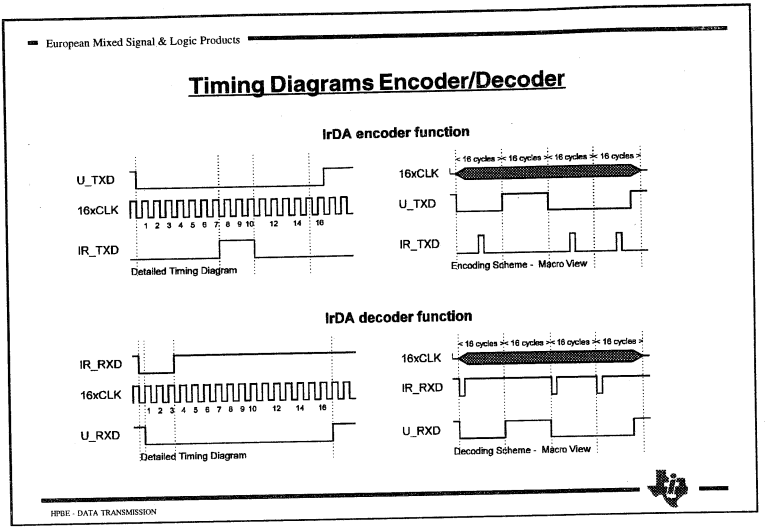
IrDA Interface Module

The picture shows the IrDA interface module which consists of the IrDA encoder/decoder and the infrared transceiver for data communication. The module can directly be connected with the IrDA PC Interface Card via the DB9S connector.

R_L in this circuit is used to adjust the current through the LED. Depending on the current to be adjusted, it varies from 3.3 to 10 Ω (4.7 Ω for 3.3 V supply and 10 Ω for 5 V supply).

R_S and C have the function of a filter network to suppress power supply noise and other disturbances. Both are strongly depending on the noise sources. Recommendation: R_S = 100 Ω, C = 4.7 µF in parallel with 330 nF ceramics.

The Rxd output of the Temic TFDS3000 infrared transceiver is an open collector output and must be connected to V_{CC} by a resistor of typical 2 kΩ.

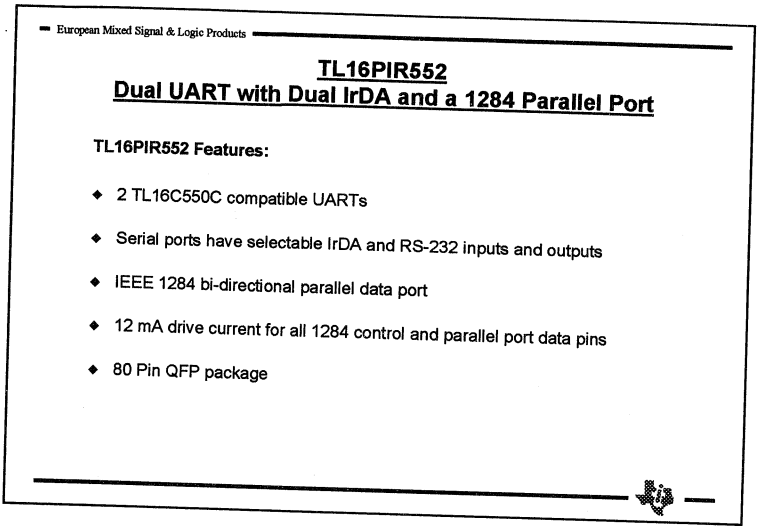


IrDA encoder function

Serial data from a UART is encoded to transmit to the opto-electronics. While the serial data input to this block, U_TXD is high (1), the output, IR_TXD goes low (0), and the counter used to form pulses on IR_TXD is continuosly cleared. After U_TXD goes low (0), IR_TXD will rise on the falling edge of the 7th 16xCLK. On the falling edge of the 10th 16xCLK, IR_TXD will fall, creating a 3 clock wide pulse. While U_TXD stays low, a pulse will be transmitted during the 7th to 10th clocks of each 16-clock bit cycle.

IrDA decoder function

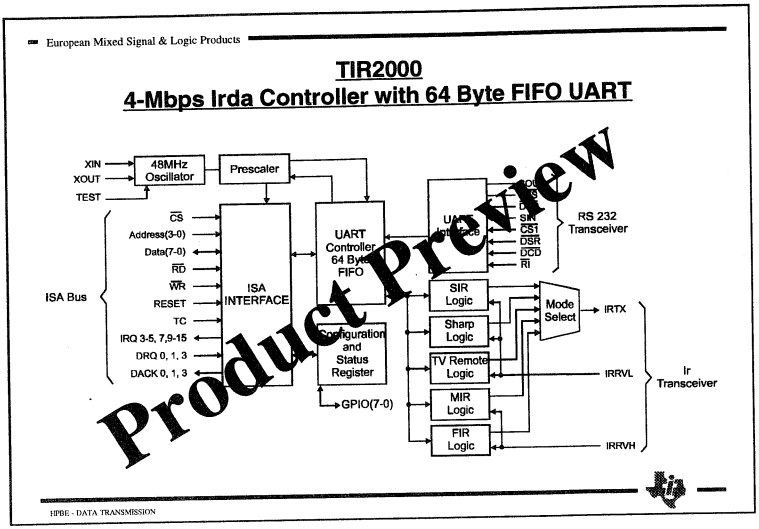
After reset, U_RXD is high (1) and the 4-bit counter is cleared. When a falling edge is detected on IR_RXD, U_RXD will fall on the next rising edge of 16xCLK with sufficient setup time. It will stay low for 16 16xCLK cycles and then return to 1 as required by the IrDA specification. As long as no pulses (falling edges) are detected on IR_TXD, U_RXD stays high.



TL16PIR552 - Dual UART with DUAL IrDA and a 1284 Parallel Port

The TL16PIR552 has a dual channel UART which is similar to the well known UART TL16C550C. These serial ports also have a dedicated infrared serial data input and the serial data outputs multiplex between a RS-232 type serial output or an infrared serial data output. This is selected through an internal register bit.

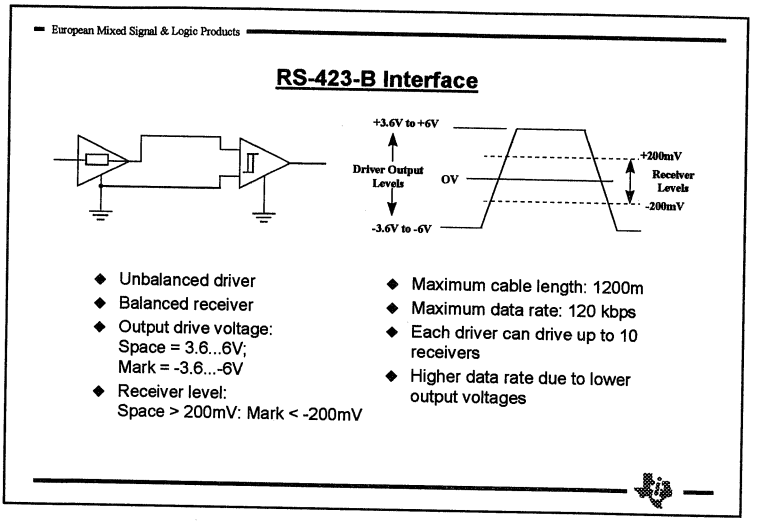
In addition to dual communication capabilities, the TL16PIR552 provides the user with an IEEE 1284 host side compatible, bi-directional, parallel data port. The parallel port will operate in compatible, FIFO, extended capability port (ECP) (with RLE data compression), and enhanced parallel port (EPP) modes. The default mode of operation is compatible with the Centronics printer port. The parallel port and the two serial ports provide IBM PC/AT -compatible computers with a single device to serve a three system port.



TIR2000 4-Mbps IrDA Controller with 64 byte FIFO UART

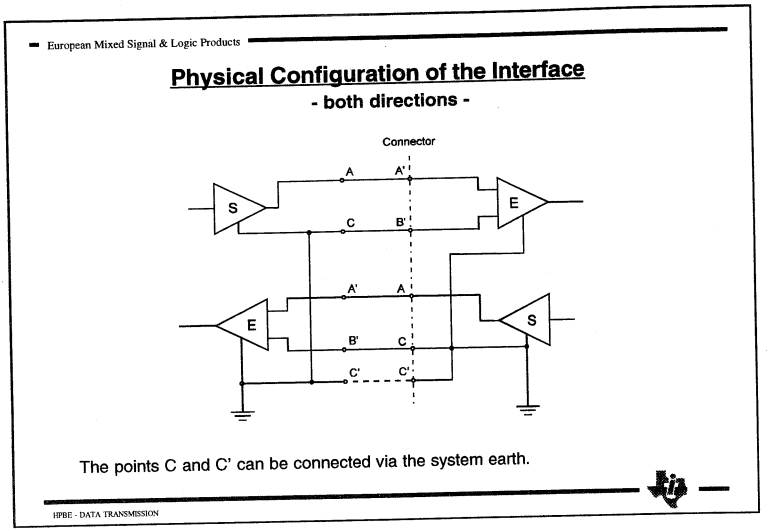
The TIR2000 is a serial communication controller with full infrared support which is also compatible to the TL16C550 and TL16C750 UART devices. This device also supports the Sharp-IR, HPSIR, MIR, FIR and TV modes. The controller has a 64 byte FIFO which reduces the CPU of excessive software overhead. Also a 64 byte FIFO meets the minimum frame size requirement which simplifies the software driver design. DMA and interrupt support for all operations have been included in this architecture. The TIR2000 offers programmable registers for routing interrupt DMA handshake signals. During the UART mode, the 65 byte FIFO and selectable auto flow-control for RTS and CTS increases system efficiency and baud rate.

- IrDA 1 mode with a data rate up to 115.2 kbps
- IrDA 1.1 mode with a data rate up to 1.15 Mbps
- IrDA 1.1 mode with a data rate up to 4 Mbps
- Sharp ASK infrared mode
- Consumer television remote control



RS-423-B Interface

The limitation on transmission distance has been partly overcome with the RS-423B interface which still uses an unbalanced line. However only one end of the transmission system is grounded preventing ground loops. The receiver side in the RS-423B is differential. The unbalanced drivers and differential receivers are used to overcome the problem of crosstalk and differing ground potentials. For RS-423B the data rate is increased to 120 kbps at around 30 metres and to 3 kbps at 1.2 km. This is mainly achieved by reducing the maximum output signal swing.

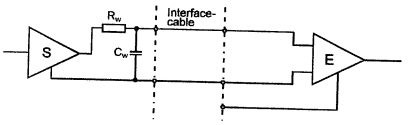


Physical Configuration of the Interface (-both directions-)

The physical configuration of the interface for both transmission directions is shown in the picture above. Care should be taken that the grounding is made seperately on driving- and receiving-side. Thus, the ground of the driver is not connected to the ground of the receiver to prevent ground loops.

European Mixed Signal & Logic Products

Circuit Suggestion for Signal Shaping



C_W µF	Data Rate kbit/s
1	0 bis 2,5
0,47	2,5 bis 5
0,22	5 bis 10
0,1	10 bis 25
0,047	25 bis 50
0,022	50 bis 100

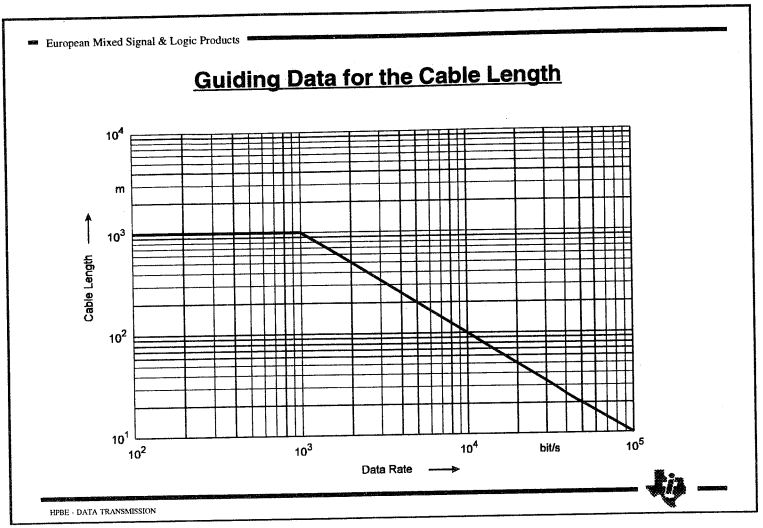
- The signal shaping limits the crosstalk in neighbouring interface cables
- Values for a cable capacitiy of 50 nF/km and a resistor, to give total resistance of 50 Ω

IPBE - DATA TRANSMISSION

Circuit Suggestion for Signal Shaping

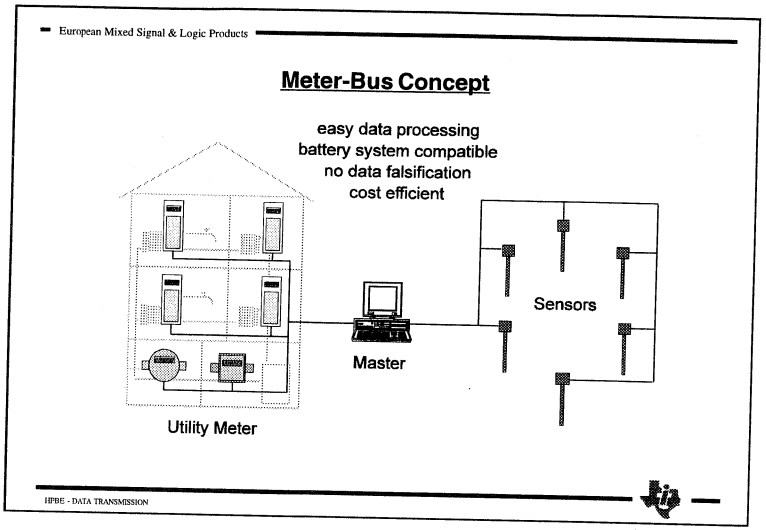
The intention of that signal shaping is to minimize the crosstalk in neighbouring interface lines. This can be achieved via a RC network as it is described in the picture above. The table gives the values for the added capacity C_W for the different data rate, if the cable capacity is 50nF/m and the resistor R_W is chosen that the resulting resistance is 50 Ω.

Another possibility is to use a RS-423B driver with a controlled driver slew rate. Texas Instruments offers the **SN75LBC784** and the **SN75LBC786**, which are quadruple RS-423B driver/receivers. The driver slew rate of these components can be controlled by a single resistor.



Guiding Data for the Cable Length

As already mentioned, the data rate for RS-423B is increased to 120 kbps in comparison to the RS-232 interface which supports only data rates up to 20 kbps. However this data rate can only be achieved at a maximum cable length of around 30 metres as it is shown in the picture above. Above this data rate the cable length drops with 20 dB/decade. At the maximum cable length of 1.2 km, the data rate decreases down to 3 kbps.



Meter-Bus Concept

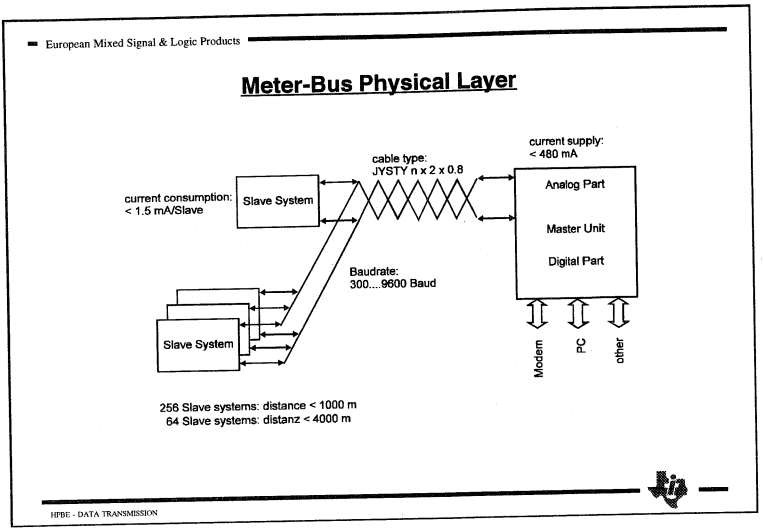
In applications like Utility Meters or remote measurement in the field the usage of battery powered sensor systems is rapidly increasing. The operation for many years with one set of battery is a basic requirement and therefore these systems are designed for very low current consumption, down to a few mircoamps.

Once electronic Utility Meters are installed in private and commercial buildings the need for a bus system is very clear. A bus system for electronic meters offer a lot of advantages. Data processing can be done very easily. Computer systems can exchange information as often as necessary and erroneous read-outs are minimised. If all meters are read-out fully automatically privacy and a maximum of security are guarantied for the end-user. No meter-man has to access private homes which is also a major cost reduction.

The bus system can connect the meters with a central Master Unit where read-out data are collected and stored and from which they can be transmitted via modem and telephone lines over long distances.

Such a bus systems used to link these meters or sensor systems and connect them to a central Master Unit have very special requirements:

- long transmission distances
- safe data transmission
- a maximum of slave count
- compatibility to other Utility meters
- no impact to the sensor system lifetime, i.e. remote power supply
- standard wiring material
- polarity independent



Physical Layer

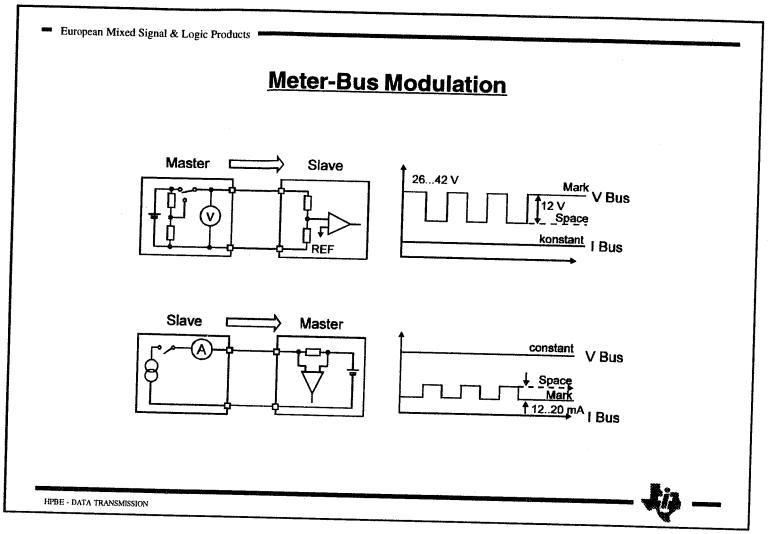
The Meter-Bus uses a Master Unit that controls the protocol on the bus as well as supplying the power for the data transmission. It consists of an analog part that is modulating the bus and detecting information sent from the slave systems.

The slaves, which are typically Meters are connected via a bus-driver unit to ordinary twisted pair telephone wiring material (called JYSTY nx2n0.8lb). For the connection the bus-driver TSS721 is used. Up to 256 slaves can be connected to one Master Unit over a maximum line length of 1000 m. This distance can even be expanded to 4000 m if not more than 64 slaves will be connected.

Each slave is identified by its unique address. The communication is bi-directional. The transmission rate is defined with 300 to 9600 Baud. The power supply for the TSS721 is provided via the bus lines. Some of the energy supplied on the bus lines (1.5 mA/slave) can be used to provide remote powering to a connected slave.

The digital part of the Master Unit controls the level on the analog part, which is handling the bus signals. It is also controlling the bus protocol and is handling data collision. The Master Unit can hold any kind of processor.

The protocol used, which is not at all defined by the Meter-Bus, defines the hardware requirements of the digital part. A Master Unit typically is equipped with an interface to other data processing or transmitting systems (like PC, Modem, Handhold Terminal, other Bus Systems).



Modulation

Since the Master Unit needs to supply the power for the driver unit as well as for the driving of information a current loop seems to be ideal. A typical current loop works with 20 mA levels. However 256 systems connected to a bus each working on 20 mA is too much power on an ordinary telephone cable type. A pure voltage modulation would require a lot of power from the slave supply system to drive the information through the lines to the Master. A remote supply would be impossible.

The Meter-Bus uses both versions. The communication from the Master to the slave is done using different voltage levels. The communication from the slave to the Master is done by different current levels.

Master to Slave

Depending on the number of slaves connected to the system and depending on how much power is used for remote power supply a certain idle current level is defined.

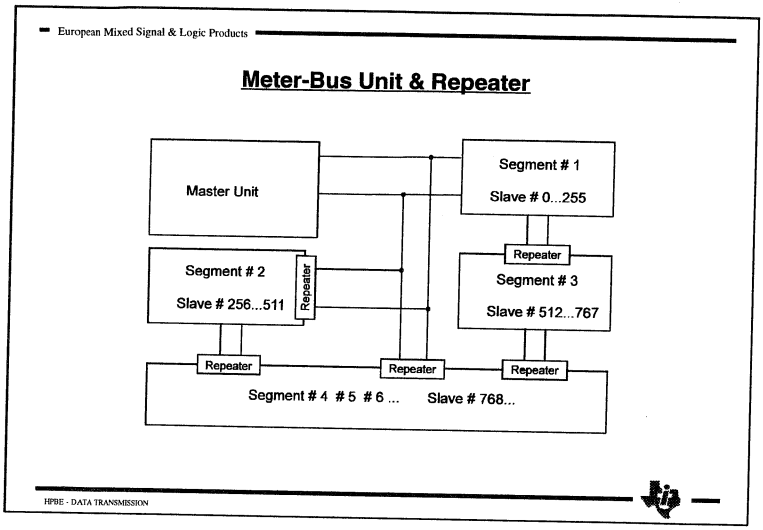
The idle mode, the mark state, is defined by a voltage level between 24 V and 42 V. A space state is defined by a voltage drop of 12 V. Whatever the mark state is in the given window, the space state is less 12 V down to 0 V. 0 V is an invalid state since the power supply on the bus would break down. The idle current remains almost unchanged during this modulation.

Slave to Master

Any slave is sending data to the Master Unit by modulating the current on the bus. Only one slave system can send at one time. Bus collision must be handled by the protocol and the Master Unit. The TSS721 driver unit activates a built-in current sink to modulate the current on the bus lines. The idle mode, mark state, is 0 mA to 1.5 mA signal level. The space state is a maximum 20 mA signal level. The signal level is defined as the current flowing without idle current used to supply the TSS721 units and the remote powered slaves. The mark level voltage remains unchanged during this data transmission.

Since the TSS721 is configured for half duplex only, the current modulation from RX or RXI is concurrently repeated as ECHO on the outputs TX and TXI. In case a slave as well as the Master is trying to send information via the bus the added signals are appearing at the outputs TX and TXI which indicates the data collision to the slave.

Because the bus is always powered during normal run mode a connected slave can send requests at any time the bus is unused and the remote power feature can be used to supply connected slaves without their own power.



Master Unit & Repeater

As already described one Master Unit can handle up to 256 TSS721 units for a maximum cable length of 1000 meters. Whenever more than 256 units are connected to the bus or the cable length is longer than 1000 meters, Repeaters are necessary. A Meter-Bus Master Unit supplies all connected slaves with power for the Driver units as well as power for the communication and, if used, with remote powering for the micro-controller system.

Each Repeater can handle maximum of 256 slave units for a bus line length of 1000 m. As many Repeaters as necessary can be used in a Meter-Bus system. A Repeater serves a segment. Up to 256 segments can be connected to one Master Unit via 256 Repeaters, and even that can be expanded if necessary. In each segment 256 slaves can be attached to the bus lines. A Repeater works similar to a Master Unit for the served segment. The input works as an input in a slave system. It detects different voltage levels and transmits these voltage levels to the connected slaves. To a Master Unit a Repeater simulates one slave load. A Repeater uses its own power supply to provide the slave systems in its segment with power and information.

A current signal on the bus lines in a segment is transferred by the Repeater to the main-bus lines connected to the Master Unit. Similar to the TSS721 driver unit the Repeater uses a current-sink to transmit information via different current levels. For the Master Unit a Repeater with its connected slaves is one slave load only.

The protocol is transparent to all connected slaves. This means for example a transmitted address is read by all connected slaves regardless to which segment they are connected. This also means that an address system must be able to address more than 256 slaves. There is no need to connect slave addresses in sequential order to one segment. Repeater and slave systems can be connected to the Master Unit in parallel as long as the maximum number of slaves and Repeaters does not exceed 256 and the maximum line length of 1000 meters is not exceeded.

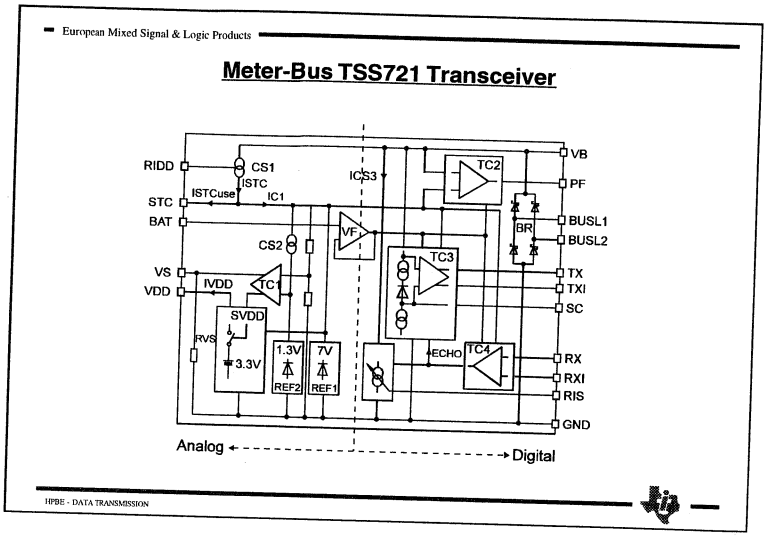
TI developed an Analog Part of a Master Unit for evaluation purpose. Since the Digital Part of a Master is basically defined by the protocol used on the bus lines, the unit is defined with an interface for any digital processing unit. Any customer will define its own Master Unit and Repeaters but all will show similar features in the Analog Part.

The TI Analog Master Unit expects a processor system that is controlling the data communication in a half-duplex mode. It is this processor system's task to include check-sums to the protocol, check data collision, store data in RAM, EPROM or other media, and control the different run modes of the connected slaves. This processor is not included in the TI evaluation unit. For an evaluation a PC might be used to install a prototype system.

The master Unit must be equipped with an isolated power supply that can supply the power for the slaves. The system must have a galvanic isolation from ground to guarantee a ground-free bus system. 256 slaves must be supplied with a maximum of 1.5 mA per slave plus additional 20 % security for short-circuits in a slave or at data collision.

Data transmission from slaves must be identified. Since all connected driver units and remote power slaves are bus-powered, this power consumption level must be identified as idle state. Only fast current changes after the bus system is powered-up are considered as data information and must be transmitted to the Digital Part. When a Master Unit can adapt to the idle current consumption of a bus, a calibration cycle is not necessary when the bus system or slave number and type are changed.

Overload and short-circuit conditions are checked to avoid the destruction of slaves systems and measurement data.



One of the major requirements for the realization of a cost efficient Bus concept is to reduce the number of electronic parts and costs for the driver interface, because the driver interface is a high volume product. The major objective of the TSS721 development was therefore the integration of all necessary functions in one IC with a minimized number of external parts.

TSS721 Features:

-receiver/transmitter logic according to the Meter-Bus specification with dynamic level recognition

-adjustable constant current sink via external resistor (nominal 20 mA according to DIN standard 66258 and 66348)

-polarity independent

-power-fail functions

-backup supply functions

-remote powering

Analog Part

The bus lines are connected to the pins BUSL1 and BUSL2. The rectifier bridge rectifies the bus voltage and makes the device polarity independent. The signal is then available at the pins VB and GND. If the chosen bus voltage is very low and the internal voltage drop can not be accepted, the bus voltage can be supplied to the driver via pins VB and GND. The voltage drop in the Schottky rectifier diodes is then eliminated, but the bus lines are no longer polarity independent.

The bus voltage supplies several constant current sources. These constant current sources are the power supply of the entire TSS721 as well as for the connected module which is remote powered. The concept to take all power supply out of the constant current source, is required by the Meter-Bus. Request is a constant quiescent current from the bus. A current variation in each connected module would be added up and cause erroneous transmission.

The constant current source CS1 is the main power supply and can be programmed by an external resistor typically in the range of 400 µA to 960 µA. The resistor connected to the RIDD pin and the current ISTC are calculated by the following formula:

$$I_{STC} = \frac{V_{RIDD}}{R_{IDD}}$$

ISTC	= constant current of CS1
VRIDD	= reference voltage on pin RIDD (typ. 1.26 V)
RIDD	= 13 k*...80 k*

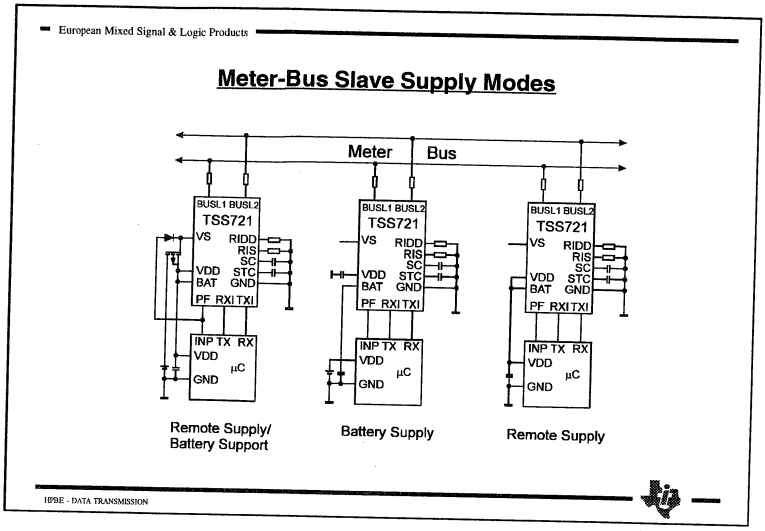
The current ISTC splits into the current for the device supply and the charge current for a support capacitor. The support capacitor provides current for a connected module at current peaks and in case the bus power fails. The capacitor is connected to pin SC.

When the bus voltage is switched on and the TSS721 is powered a certain time is required to charge the support capacitor. Since the load current is limited it may, in some cases, take up to one minute until the TSS721 starts the initialisation routine. REF1 tracks a capacitor voltage of typical 7.0 V and activates a Zener diode to take additional current. As already described a constant load on the bus is mandatory.

TC2 tracks the bus voltage and in case of a power-fail pin PF is activated. This pin may be used to detect a power failure and initiate a safe shutdown of the micro-controller system. During the shutdown, power can be supplied by the support capacitor. In case the capacitor voltage falls below 7.0 V the comparator TC1 switches off SVDD since it is not possible to regulate the voltage on VDD to a constant level of 3.3 Volts any longer. Than the low-active pin VS can be used to control a FET-switch which may activate a support battery.

Digital Part

The signal TX and TXI, the inverted output, generate a digital output depending on the voltage levels on the bus. A mark state generates a high level that is defined by the BAT input, the supply voltage of the slave system. The RX pin, or the inverted input, activate the current sink in case the slave system needs to send a logical high. The level acknowledgement is again controlled via the input BAT. RIS is a control input and must be always connected to ground, via a resistor.



The TSS721 utilize three different energy supply modes for the connected slave systems. The three modes are:

-Local Supply :	energy for slave supplied locally, i.e. by battery
-Remote Supply:	energy for slave supplied by the bus
-Mix Mode :	energy for slave supplied by bus, in case of power-failure a backup battery is activated

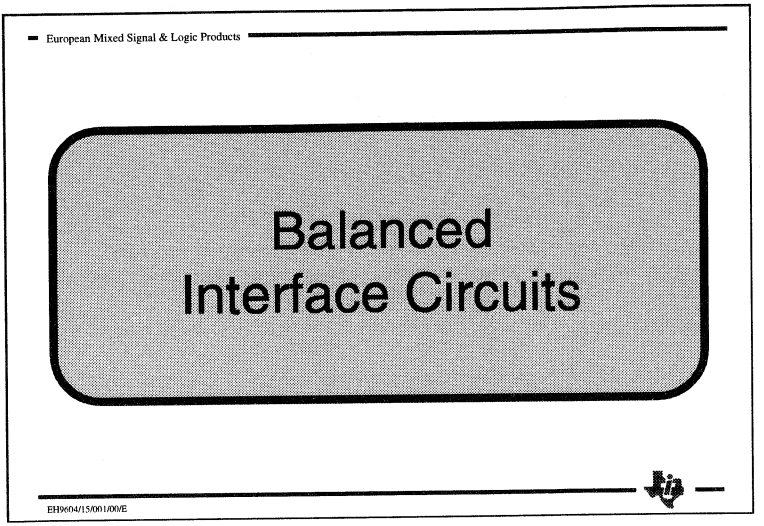
When power for the slave is supplied locally, normally by a battery, the TSS721 is working as a pure driver device only. The information on the bus is supplied in the right voltage format to the slave system. The communication initiated by the slave micro-controller system is transferred into current modulations. For security reasons it is advisable to add resistors (430 Ω) between the bus lines and each driver device. Using resistors has the additional feature that in case of a short circuit the additional power consumption can be tracked by the Master Unit that can initiate an alarm.

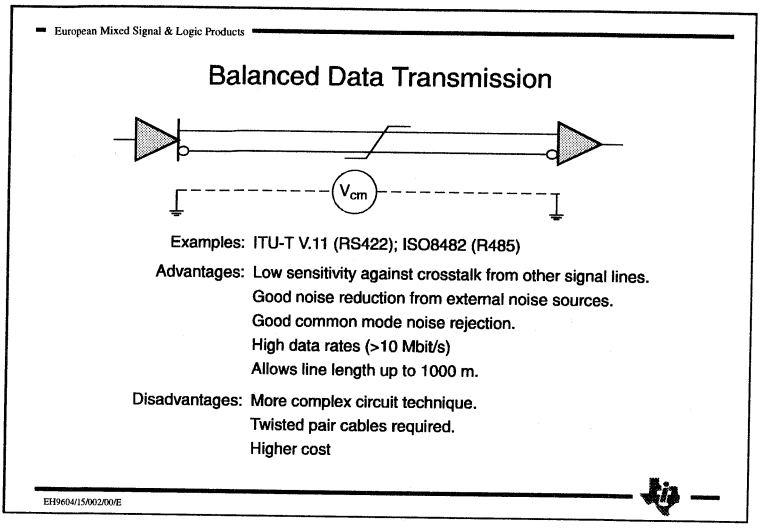
Even though the defective unit can not be addressed any longer, all other devices connected to the bus can still be accessed.

The TSS721 allows the remote power supply for the slaves. The driver unit performs the data transmission and the module is fully powered by the bus. In case of a voltage breakdown on the bus the power-fail signal is activated. This enables the processor to save important data and initiate a safe shutdown. The power for this is delivered by the support capacitor.

In the mix-mode the slave system is supplied by the bus lines as long as power is available. A power failure is also indicated by the power-fail pin PF. Additional to this a backup battery is activated by a FET-switch, controlled by the VS pin. The backup battery is active during the bus-off time only so the power supply for the slave system is guaranteed. Since the power-fail pin is still usable for the application to track the power failure, a low power consumption mode can be started. Thereby the capacity of the backup battery may be minimized.

In all three supply modes the TSS721 is powered by the bus lines as long as no power-fail occurs and it does not use any slave system battery capacity.


European Mixed Signal & Logic Products
Balanced
Interface Circuits
EH9604/15/001/00VE

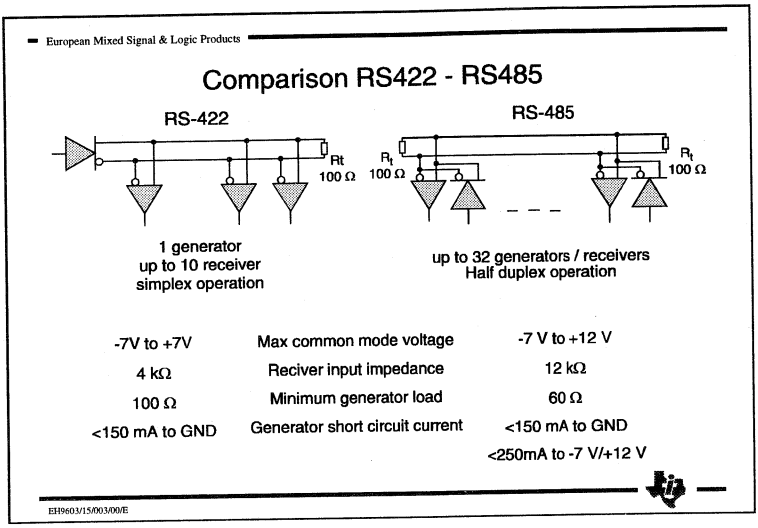


Balanced Interface Circuits

Balanced Data Transmission (15002)

Balanced interface circuits consists of a generator with differential outputs and a receiver with differential inputs. Under the assumption that any noise is coupled into both wires of the transmission line in the same way, the voltage difference between these two wires will be always zero. Due to the common mode rejection capability of a differential amplifier this noise will be rejected. This is true in any case for crosstalk from neighbouring signal lines. It is also true for noise from other noise sources as long as the common mode voltage goes not beyond the common mode range of the receiver. The common mode rejection of the receiver eliminates also to a certain degree noise caused by a ground voltage difference between the generator and the receiver. The twisted pair cable used in these interfaces in combination with a correct line termination - to avoid line reflections - allows very high data rates of more than 10 MBit/s and a cable length of up to 1000 m.

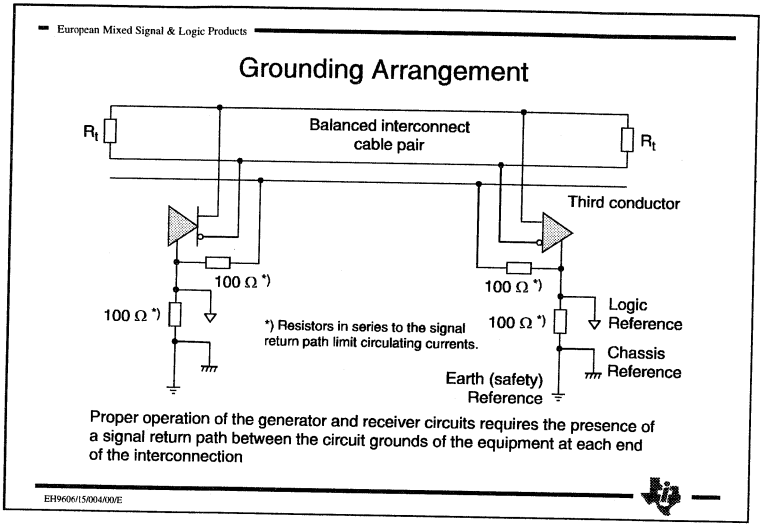
All these advantages come with some drawbacks. Due to the more complex circuit technique required to achieve the high performance these circuits are more expensive. Furthermore the high data rate possible requires well defined line impedance and a correct line termination to avoid line reflections. Also twisted pair cable instead of cheap multi core cables have to be used.



Comparison EIA-RS422 - EIA-RS485 (15003)

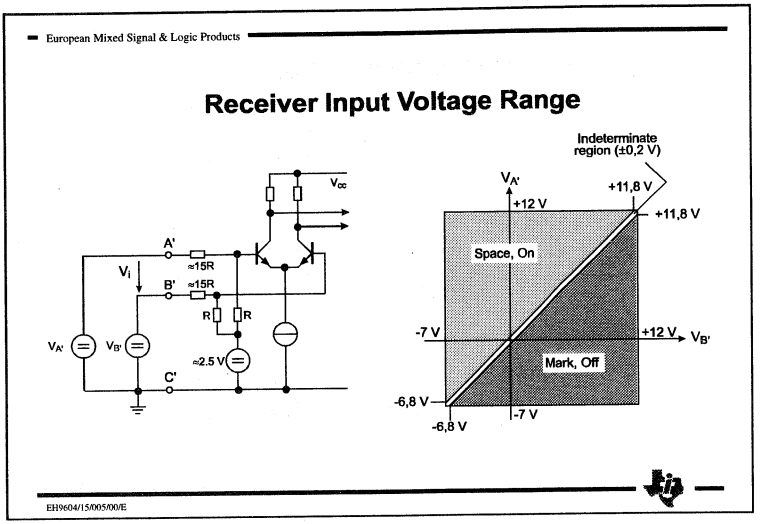
There are two standards often referred to which describe balanced interface circuits: EIA-RS422 (international standard ITU-T V.11) deals with a point to point interface where up to 10 receivers may be connected to one generator. The limiting parameter for the number of the receivers is the input impedance R_i = 4 kΩ of these circuit. The total load of 10 receivers R_{itot} = 400 Ω plus the impedance of the mandatory termination resistor R_t = 100 Ω is the maximum load to the generator. The standard EIA-RS485 (international standard ISO 8482) describes a balanced interface. Due to the higher input impedance of the receivers/transceivers in this standard (R_i = 12 kΩ) up 32 transmitter, receivers, transceivers or any combination of them can be connected to the interface. Owing to the bi-directional data transfer, the line has to be terminated by an appropriate termination resistor at both ends.

The common mode voltage between the various station is allowed to be up to ±7 V. Note that EIA-RS422 specifies the maximum common mode voltage V_{cmmax} = -7 to +7 V, while EIA-RS485 specifies the maximum input voltage range (common mode voltage plus signal voltage swing) V_{imax} = -7 to +12 V. On interfaces with long transmission line the circuits have to be protected against a short circui. In a point-to-point interface a short circuit between the two signal lines, or to GND has to be considered. The short circuit current under this condition is $I_{os} \leq$ 150 mA. In a multi-point interface the common mode voltage V_{cm} = ±7 V has to be considered, too. Therefore the short circuit current to a voltage applied to output of V_o = -7 to +12 V will be $I_{os} \leq$ 250 mA.



Grounding Arrangement (15004)

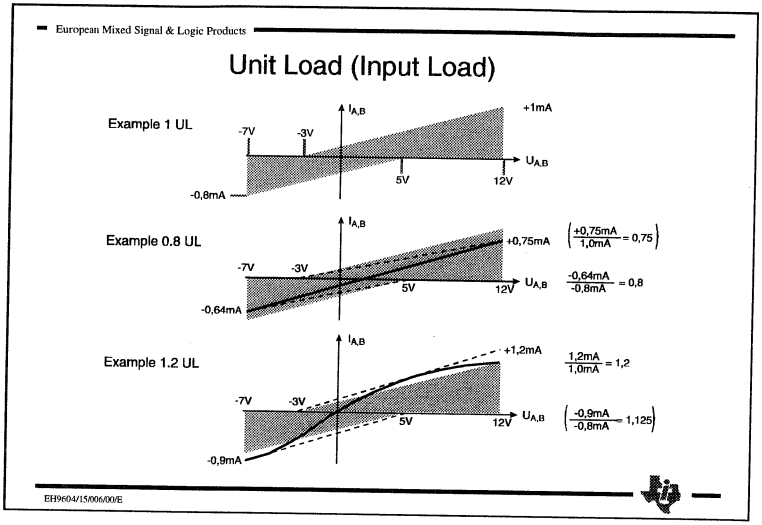
Proper operation of the generator and the receiver requires the presence of a signal return path between the circuit grounds of the equipment at each end of the interconnection. The circuit reference may be established by a third conductor connecting the common leads of the devices, or it may be provided by the connection from each equipment to an earth reference. Where the circuit reference is provided by a third conductor, the connection between circuit common and the third conductor must contain some resistance (e.g. 100 Ω) to limit circulating currents when other ground connections are provided for safety.



Receiver Input Voltage Range (15005)

As already mentioned, the receiver is built up by using a differential amplifier construction (see the simplified circuit diagram above). To achieve a large common mode range (larger than the supply voltage of the circuit V_{cc} = 5 V) the input voltage is divided by a voltage divider by a factor of ≈ 15. The other end of this resistor divider is connected to an internal reference voltage of about 2.5 V. With an input voltage varying between -7 V and +12 V, the voltage at the input of the differential amplifier (the bases of the two transistors) will vary between about 1.5 and 3.5 V. Such an input voltage will guarantee sufficient margin for a correct operation of the differential amplifier supplied by a supply voltage of 5 V alone.

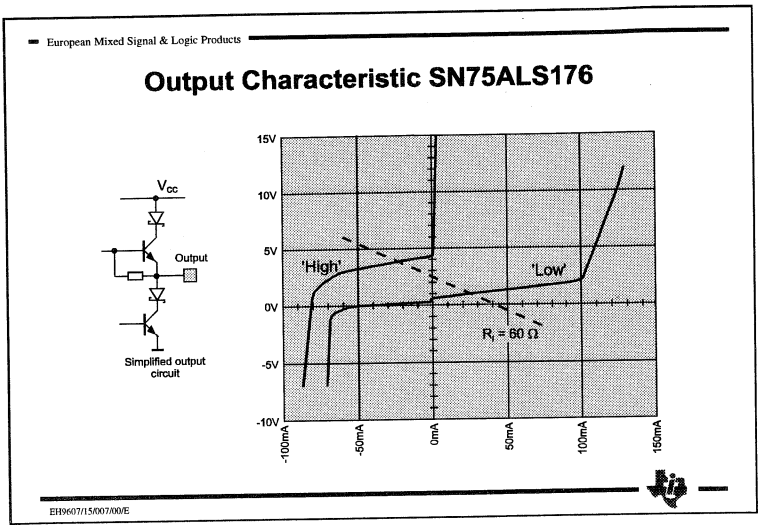
The sensitivity of the differential amplifier measured at the resistor divider input is 200 mV. Any differential input voltage V_i = 0.2 to 19 V will represent an On voltage, while an differential input voltage V_i = -0.2 to -19 V will represent an Off voltage. The output of the receiver is forced to the corresponding logic states.



Unit Load (15006)

The receiver's input impedance determines the maximum number of circuits that can be connected to a generator. Since semiconductor components like the receivers discussed here have mostly a non-linear characteristic, is it not possible to specify the input impedance of such a circuit by a simple resistor value. Instead a so-called Unit Load has been specified which defines an area in which the curve input characteristic has to fit. One unit load (UL) is determined - as the picture above shows - by the corners 12 V / 1 mA and -7 V / -0.8 mA. Such a load represents a resistor of 12 kΩ. The input impedance of the receiver may be higher or lower than this value. Many advanced interfaces for example show a higher input impedance. The middle example in the picture represents a circuit with 0.8 unit load only. In this case the maximum number of receivers connected to the interface can be increased according to the lower load of the circuits.

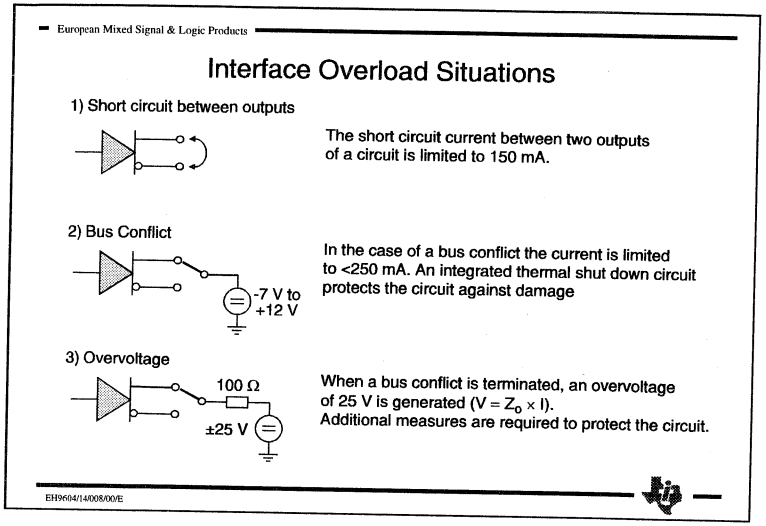
As already mentioned, semiconductor components mostly show a non linear characteristic. To determine the unit load of such a circuit one draws the input characteristic in the unit load diagram and adds a line starting from the point -3 V / 0 mA to positive voltages to be the tangential to the input characteristic. Where this line reaches the input voltage $V_{A,B}$ = 12 V, one gets the corresponding input current $I_{A,B}$. The ratio between this input current and the input current of 1 UL gives the unit load of the circuit in question. This analysis has to be done for the positive as well as for the negative current. The greater of the two unit loads found determines the final unit load of the circuit. (see the example in the diagram above)



Output Characteristic (15007)

Generators in balanced interface circuits have a similar output circuit to bipolar logic circuits. However a few modifications have been added not required in simple logic components. First, the generator output circuit contains two additional Schottky diodes as shown in picture above. These diodes allow us to apply voltages to the output which are more positive than the V_{cc} terminal or more negative than the GND terminal. The diode in series with the upper output transistor blocks the reverse current in this transistor and avoids a breakdown of the base-emitter diode, when a high positive voltage is applied to the generator. The diode in series with the lower output transistor prevents the parasitic diode in parallel to this transistor conducting when a negative voltage is applied to the circuit.

Not shown in this simple diagram are measures to limit the output current under overload conditions. However the diagram shows that the short circuit output current of the device is I_{osL} = 100 mA and I_{osH} = 80 mA. The diagram shows also that the short circuit current will be limited over the full output voltage range V_o = -7 V to 12 V. The typical output current under operation (assuming an output voltage V_o = 3 V and a load R_L = 60 Ω) is only I_o = 50 mA.



Interface Overload Situations (14008)

In interfaces which are distributed over a large area the system designer has to take care of the various overload conditions which may occur during the operation of the system:

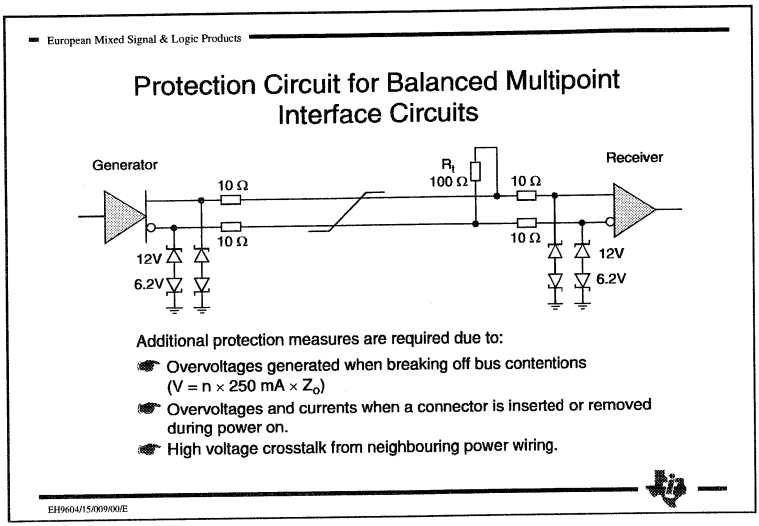
1) Short circuit between the two outputs of a generator: As already mentioned, the generator output circuit has a built in current limiter which limits the output current to a maximum short circuit current $I_{os} = \pm$ 150 mA. Such a short circuit may last for a unlimited time.

2) In a multi-point interface two or more generators may be active simultaneously. Under these circumstances, we need to consider a ground potential difference (common mode voltage) $V_{cm} = \pm$ 7 V. At first, owing to the higher voltage across the output circuit, the current may increase up to $I_{os} = \pm$ 250 mA. The previous diagram shows a certain dependency of the short circuit output current on the output voltage. Since the voltage drop across the output circuit is now the sum of the output voltage V_o and the common mode voltage V_{cm}, the total power dissipation in the output circuit will be:

$$P_o = (V_o + V_{cm}) \cdot I_{os} = (5V + 7V) \cdot 250mA = 3W$$

To prevent a destruction of the circuit, a thermal overload circuit is integrated, which turns off the output circuit when the chip temperature reaches a certain limit and re-activates the output after the chip temperature has fallen down to an normal value. This measure again allows an unlimited short circuit even under a bus contention situation.

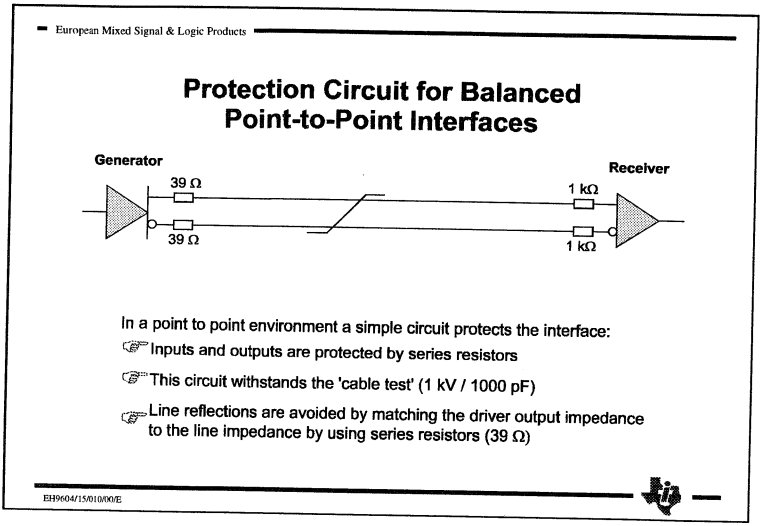
3) When a bus contention is terminated, the current in the line is turned off. This change of current will cause an overvoltage $V = Z_o \times I_{os}$. This condition may cause an overvoltage of up to 25 V. The design engineer has to take measures to protect the interface from this voltage.



Protection Circuit for Balanced Multi-point Interface Circuits (14009)

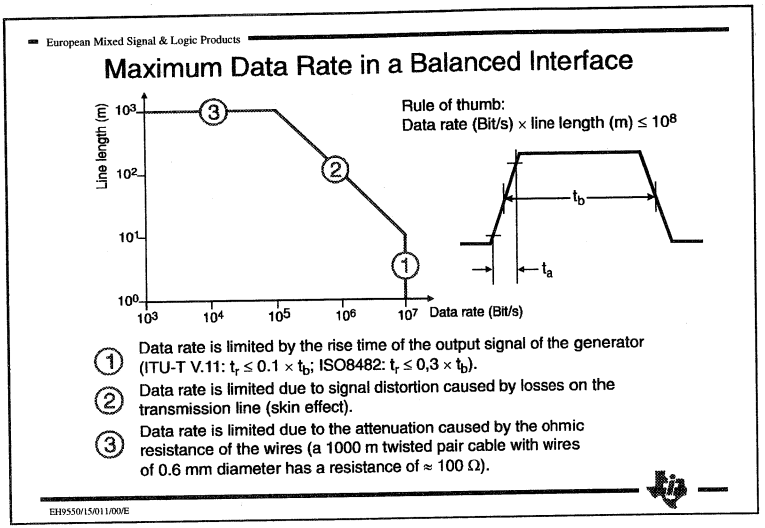
Another cause of destruction of the generators and the receivers is the insertion and removal of the connectors while the supply voltage is on ('hot plugging'). Due to the random sequence of connecting the contacts of the connector a very high current e.g. caused by the ground potential difference between the circuits may flow into the inputs and outputs of the integrated circuits. This high current will damage the interface. To protect the interface a combination of zener diodes (to limit the voltage) and series resistors (to limit the current) is recommended. Such a circuit protects the interface also against high noise voltage caused by crosstalk in a noisy environment.

It has to be mentioned, that this protection circuit influences the characteristic of the interface. The series resistors increase the output impedance and lower the voltage swing of the generator. This effect may cause a problem with long transmission lines where the line losses have to be considered. The zener diodes have a very high capacitance which slows down the signal slew rate and by this the maximum data rate.



Protection Circuit for Point-to-Point Interfaces (14010)

In point-to-point interfaces simple protection measures are often sufficient. Resistors in series to the generator output limit the current into these terminals. These resistors also match the generator output impedance of the line impedance, so that at the line end no termination is required. The protection circuit at the receiver input consists again of series resistors. Since the input impedance of the receiver is >10 kΩ, these resistors can be in the kiloohm range. These measures in most applications avoid interface destruction during 'hot plugging' or in a noisy environment.



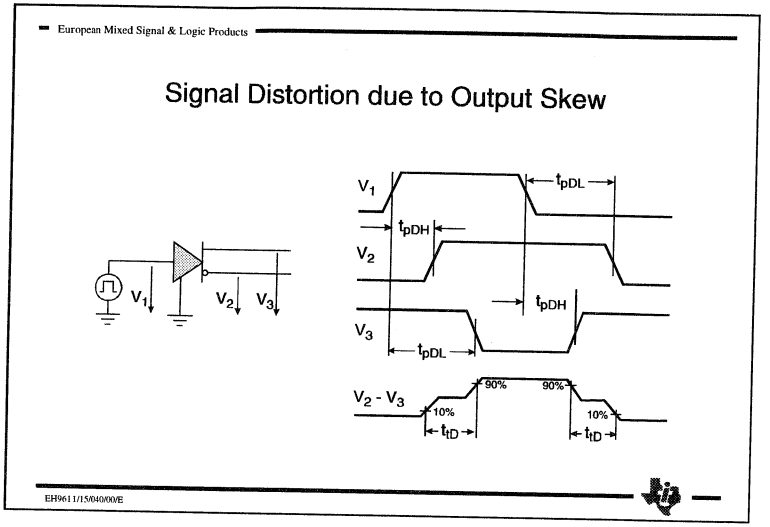
Maximum Data Rate in a Balanced Interface (15011)

The maximum data rate in an interface is determined by various parameters. The standards prescribe a certain rise/fall time of the signal to be transmitted in order to ensure a low signal distortion. The standard ITU-T V.11 allows the rise/fall time to be ≤ 10 % of the bit duration, while the standard ISO 8482 allows a rise/fall time ≤ 30 % of the bit duration. The rise/fall time of the signal is determined by the performance of the generator as well as by the losses of the transmission line. In ITU-T V.11 a diagram is shown (see the above picture) where the maximum data rate in an application can be taken from:

1) The maximum data rate at short lines (where the losses of the transmission line can be neglected) is determined by the capability of the generator. The standard recommends 10 MBit/s, while today's fast interface circuits like the SN76ALS176 can be operated at data rates up to 25 MBit/s.

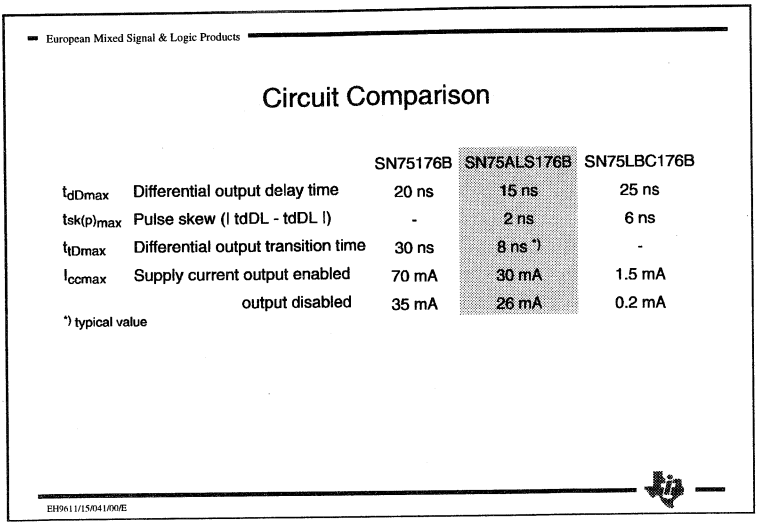
2) When the line length becomes longer than 10 m, the losses of transmission lines have to be taken into account. Therefore with increasing line length the data rate has to be reduced. A rule of thumb says, that the product of data rate (Bit/s) and line length (m) has to be ≤ 10^8. According to this formula a line length of 100 m would result in a maximum data rate of 1 MBit/s. Note, however, that this formula refers to twisted pair cable of standard quality. High quality cables will allow higher data rates.

3) Finally at long lines the ohmic resistor of the cable and the resulting attenuation of the signal is limiting as well the data rate as well the line length. The maximum line length is determined by an ohmic resistor of the cable which is about equal to the line impedance (≈ 100 Ω). A twisted pair cable with a diameter 2 × 0,6 mm and a line length of about 1000 m has an ohmic resistor of 100 Ω.



Signal Distortion due to Output Skew (15040)

Beside the distortion caused by the losses of the transmission line the design engineer has also to take care of the signal distortion caused by the generator circuit. The propagation delay time of an integrated circuit is typically different for the positive and the negative edge at the output of the device. This is caused by two reasons. First due to a different internal path length (number of inverters, gates in each path) the signal propagation time may be different. Second due to the asymmetrical structure of a bipolar totem pole output stage the rise time of the positive edge may be different from the fall time of the negative edge. The sum of these differences in propagation time is called skew. The picture above shows the result of such a skew. Since the two outputs switch at different time, the output signal "V_2 - V_3" - which is the sum of the two outputs V_2 and V_3 - initially shows only half the desired voltage swing, until the second output switches. The resulting signal distortion slows down the effective rise/fall time of the signal and thus reduces the maximum data rate.



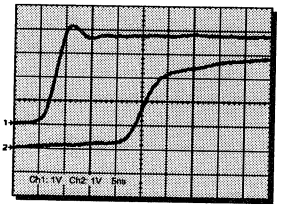
Circuit Comparison (15041)

The effort of a semiconductor manufacturer is directed in two directions: low power dissipation and high speed. Often it is difficult to combine both features in one component. As typical representatives for interface circuits, consider SN75ALS176 and SN75LBC176. The bipolar circuit SN75ALS176 has been designed for high speed applications. Therefore the propagation delay time and the skew is very short, with a penalty of a high power dissipation. The BiCMOS circuit SN75LBC176 has been designed for applications where a low power dissipation (supply current) is of concern. The disadvantage of this technique is a longer propagation delay time, a greater skew, and finally a lower maximum data rate.

European Mixed Signal & Logic Products

Signal Distortion

With longer lines and high data rates the losses (ohmic resistance, skin effect) have to be considered. These frequency dependent losses slow down the rise time of the signal and thus the maximum data rate.



Note: Signal propagation time not correctly shown

Beginning of line: t_r = 3 ns
End of line: t_r = 10 ns
Line length: l = 20 m

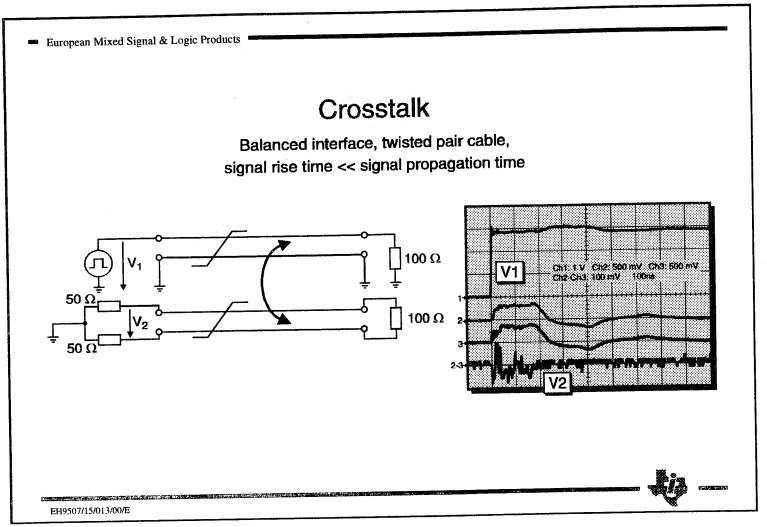
RS422: $t_b \geq 10 \times t_r$
Minimum bit duration = 100 ns
Maximum data rate = 10 MBaud

RS485: $t_b \geq 3 \times t_r$
Minimum bit duration ≤ 1/30 ns
Maximum data rate = 33 MBaud

EH9606/15012/00/E

Signal Distortion (15012)

Beside the distortions caused by the integrated circuits itself, distortion arises from transmission line losses. As discussed, the skin effect makes the transmission line act as a low-pass filter. Such a low pass filter slows down the rise time of signal and by this limits the maximum data rate. The behaviour of a twisted cable has been measured. It was found that when a signal with a rise time t_{rb} = 3 ns was applied at the beginning of the line, the rise time at the end of the line is t_{re} = 10 ns. The standard ITU-T V.11 (EIA-RS422) requires the signal rise time to be 10 % of the rise time. With a signal rise time of 10 ns the maximum data rate will be 10 MBaud. The standard ISO 8482 (EIA-RS485) allows a larger signal distortion and the rise time to be up to 30 % of the signal rise time. Using the same rise time as in the previous example the maximum data rate will be 33 MBaud.



Crosstalk (15013)

In theory in a balanced interface the crosstalk between two adjacent signal lines should be zero. Assuming a symmetrical arrangement the crosscoupled signal will be coupled into to both lines with the same amplitude. The resulting voltage difference at the affected line should be zero. The picture above shows the measurements results when an unbalanced twisted pair cable couples into a balanced circuit. The first result is that the asymmetrical noise voltage (measured between the signal line in question and ground) is about 10 % of original noise voltage. The pulse width of the noise is again twice the propagation time of the signal on the transmission line. These results have been already predicted during the theoretical analysis of the nature of crosstalk. This voltage is the common mode voltage to be rejected by the receiver. The final voltage difference between the signal lines depends on the symmetry of wire arrangement. In the best case it should be zero. Due to shortcomings of the measurement set up some differential noise voltage is found.

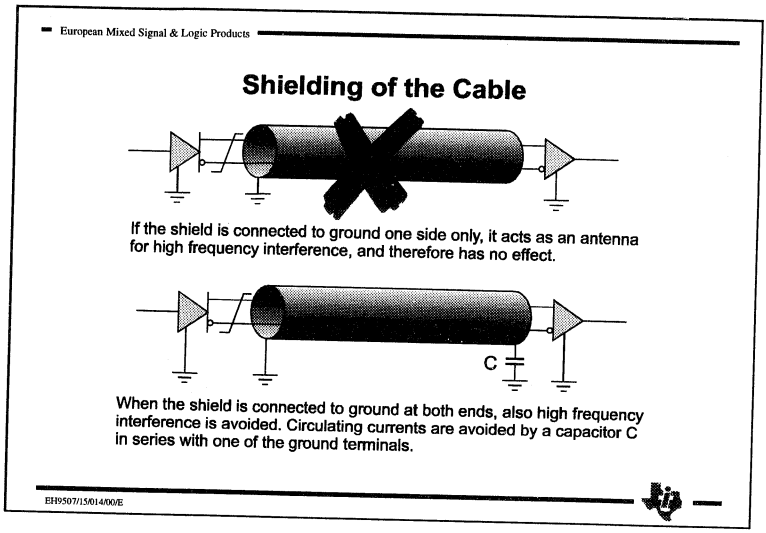
From this measurement set up a rule of thumb on crosstalk can be derived:

1) The crosstalk from any noise source into a asymmetric transmission line is about 10%.

2) The common mode voltage in a balanced interface caused by any noise source is about 10 % of the noise voltage.

3) The differential noise voltage is typically a factor of 10 smaller than the asymmetrical noise voltage.

The numbers given here apply not only to crosstalk between signal lines, but also for crosstalk between power cables and signal lines.



Shielding of the Cable (15014)

To reduce the noise coupled into a transmission line shielding recommended. However several rules have be applied to guarantee effective shielding and to avoid the shield itself coupling more noise into the interface than would happen without a shield.

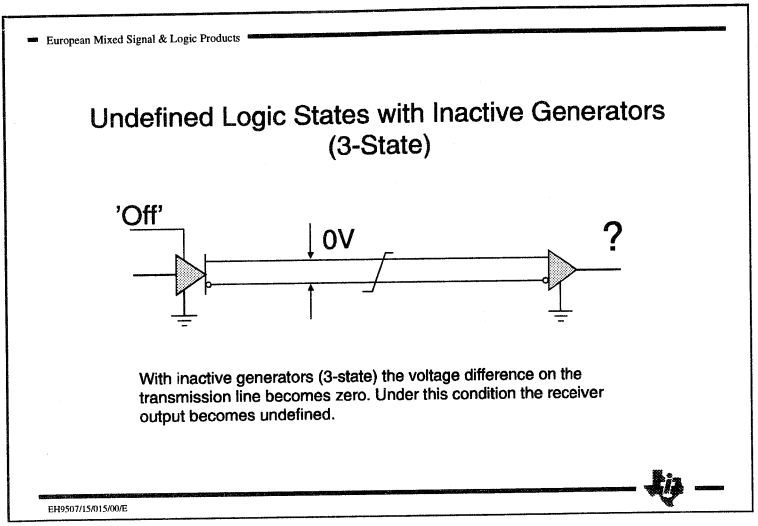
1) The shield has to be connected, at least for high frequencies, via a short circuit to the interface to be shielded. If not connected properly the shield will act as a coupling capacitance between the noise source and the circuit to be protected. In this case a shield is making the situation worse.

2) The shield has to be connected at both ends to the reference terminal of the circuit to be protected (usually ground). Otherwise the unconnected end of the shield will be an antenna which takes all the noise from the neighbourhood and couples it into the circuit.

3) The shield has to be connected seamlessly to the connector shield and to the equipment cabinet. Avoid 'pig tails' when connecting shields.

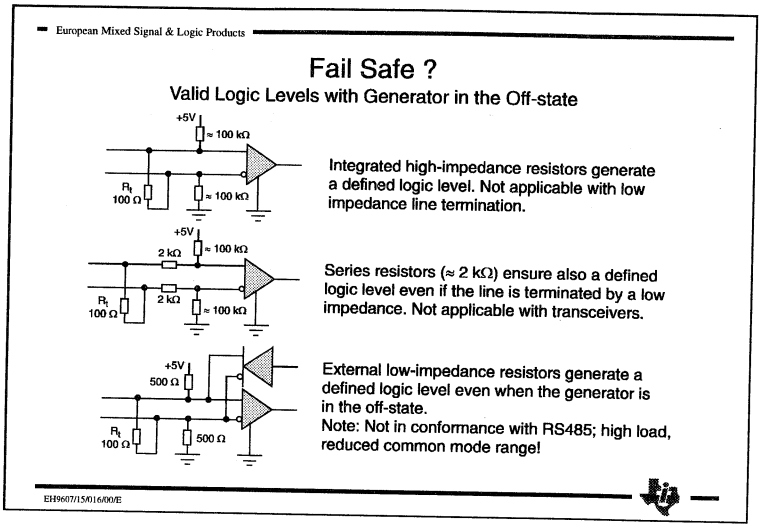
4) If the shield has to be connected to safety ground on both ends and circulating currents are of concern, a capacitor between the shield end and ground blocks these currents.

5) Single ended shields are only useful in some low frequency (e.g. audio) application.



Undefined Logic States with Inactive Generators (15015)

In multi-point interface, when all generators are switched into the inactive high impedance state (3-state) the differential voltage on the transmission line will be zero. A voltage of zero is an undefined state in such an interface. Refer to the input sensitivity of a receiver: $\Delta V_i > 200$ mV. In the corresponding standards the user will only find information that such a situation may occur and must take measures to avoid an undesired reaction of the system. Some of these measures will now be discussed.



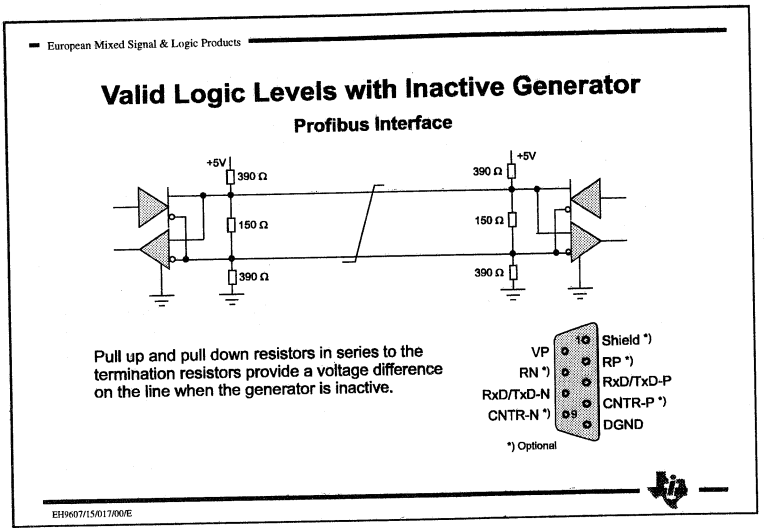
Fail Safe? (15016)

The following measures are recommended to avoid undefined states in a multi-point interface:

1) The standard ITU-T V.11 (point-to point interface!) recommends a high impedance pull-up and pull-down resistor at the receiver inputs. The intention of this circuit is to provide a defined logic state in case of a broken wire or a missing transmission line. If however the line is terminated at the end by a low impedance resistor $R_t \approx 100\ \Omega$ (mandatory in a multi-point interface!), these resistors are shorted by the termination resistor and the voltage difference becomes zero again. Interface circuits which incorporate these high impedance resistors are often called 'fail safe' in the data sheet.

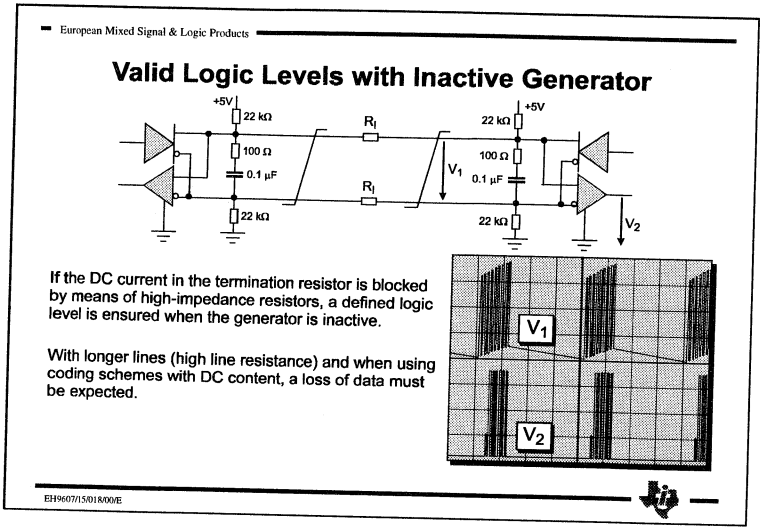
2) Another recommendation asks for additional resistors of $\approx 2\ k\Omega$ in series to the inputs. These resistors will avoid a short circuit of the pull-up / pull-down resistors even if the line is terminated by a low impedance resistor. In any case these additional resistors reduce the sensitivity of the receiver. Finally, this method is not applicable to transceiver circuits.

3) A third circuit uses low impedance pull-up and pull-down resistors ($R = 500\ \Omega$). Even if the line is terminated, the termination resistor will not short this biasing network. Therefore a differential voltage of about 500 mV stays on the line when all generators are in the 3-state mode. A disadvantage of this circuit is the load generated by the pull-up and pull-down resistors. This load reduces the maximum number of receivers connected to the interface and also influences the common mode range (high current in the resistors during a high ground potential difference between the generator and the termination circuits.)



Valid Logic Levels with Inactive Generator (15017)

The Profibus (DIN 19245) has been designed for industrial control applications. To ensure valid logic levels when all generators are in the 3-state, pull-up and pull-down resistors are placed at the line end (390 Ω each at both ends of the interface). Since these resistors are in parallel to the termination resistor, the termination resistor can be higher impedance (R_t = 150 Ω). That compensates the load of the biasing circuit.



Valid Logic Levels with Inactive Generator (15018)

An elegant method to eliminate the DC current in the termination resistor and to reduce the power consumption of the interface is to place a capacitor of 0.1 µF in series with the termination resistor. When doing this, the pull-up / pull-down resistors, which ensure valid logic levels with inactive generators, can be made high impedance (typ. 22 kΩ). The biasing function can be performed well with this arrangement. However problems may occur with the high ohmic resistance of long transmission lines. When all generators are in 3-state, the capacitors in series with the termination resistors are charged up via the pull-up / pull-down resistors to a voltage equal to V_{cc} = 5 V. When a generator now becomes active again, this capacitor has to be discharged again (average voltage at the capacitor is 0 V when the bus is active). During this discharge the voltage divider caused by the ohmic resistor of the wires and the termination resistor in conjunction with the capacitor perform a low-pass, which prevents valid logic levels at the line end for some time. As the oscillogram shows, this phenomenon leads to loss of the first part of the transmitted data stream.

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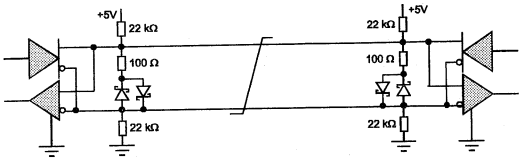
Valid Logic Levels with Inactive Generator

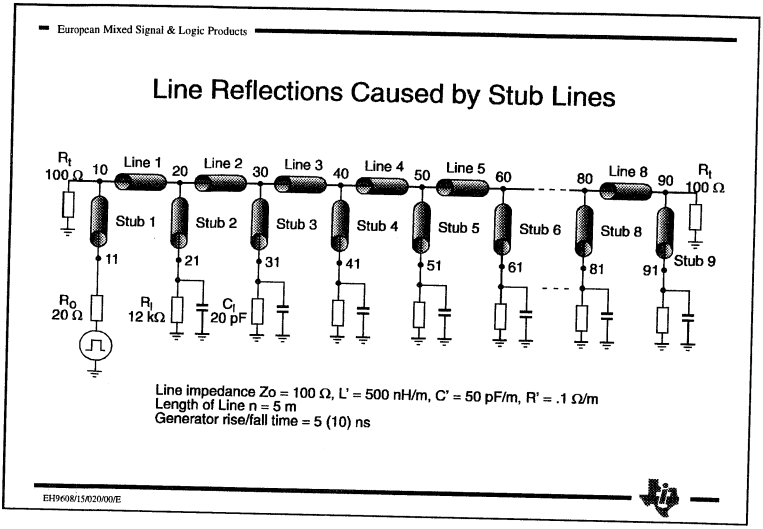


Two inverse parallel connected diodes in series to the termination resistor ensure an offset voltage >400 mV if the generator is in the inactive state (3-state).

EH9607/15/019/00/E

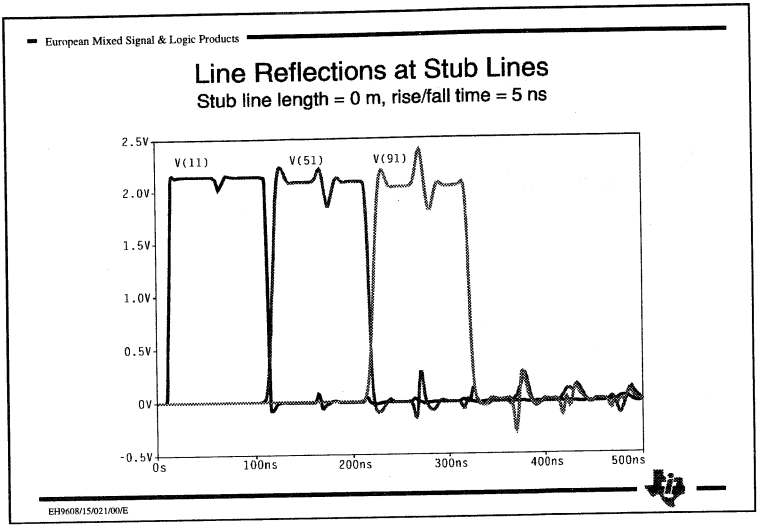
Valid Logic Levels with Inactive Generator (1501)

Adequate biasing of an inactive interface can also be made by two inverse-parallel connected Schottky diodes (forward voltage $V_f \approx 400$ mV) in series with the termination resistor. Since only a very low current is required to force a voltage drop of 400 mV at the Schottky diodes, the pull-up and pull-down resistors can be made high impedance again (22 kΩ each).



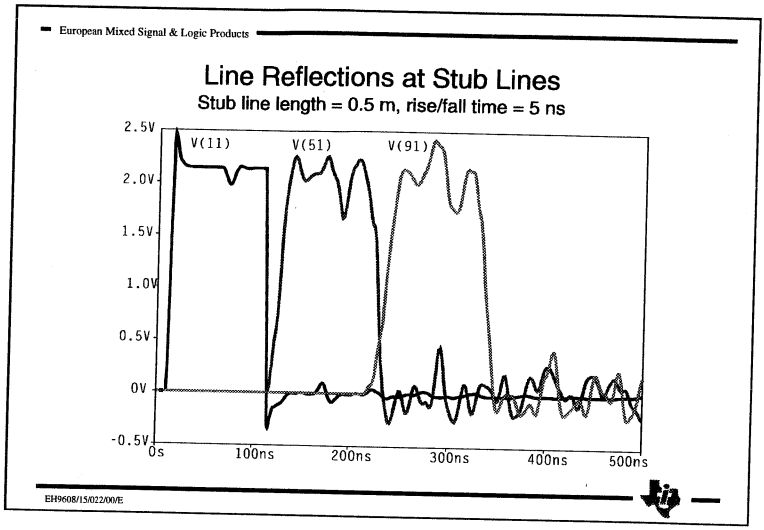
Line Reflections Caused by Stub Lines (15020)

In large networks, due to physical restrictions, it is often not possible to connect all generators and receivers directly to the trunk cable. In this case the equipment is connected via a stub line to the trunk cable. The trunk cable is terminated (as already discussed) at both ends by the correct termination resistor. The stub lines however are terminated at the ends by the high input impedance of the generators, receivers, or transceivers. The typical equivalent circuit diagram for these circuits is a resistor R_i = 12 kΩ in parallel to a capacitor C_i = 20 pF. Each high impedance termination of a stub line is a point of discontinuity which generates line reflections. The influence of stub lines and the resulting line reflections were investigated using a simulation program (Spice). In the circuit investigated the trunk cable had a total length of eight times 5 m. Every 5 m a stub line was connected. Each stub line was terminated by resistor-capacitor combination representing the input of an equipment. By varying the stub line length the signal wave-form has been analysed.



Line Reflections Caused by Stub Lines (15021)

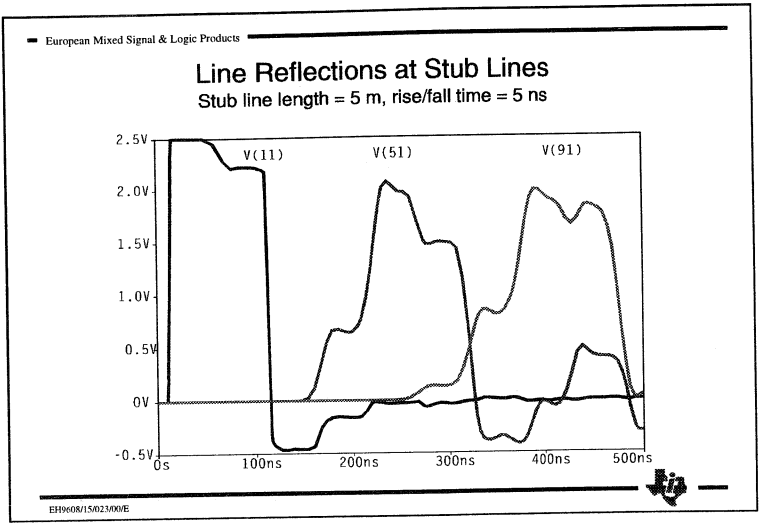
With a stub line length of 0 m, the trunk cable is loaded every 5 m only by the resistor-capacitor combination representing the generators / receivers. The high impedance of the resistor has no influence. The capacitor generates a small discontinuity, which results in small signal distortion as the picture above shows. The three signals shown are taken at node 11 (generator output), node 51 (distance on the trunk cable 4 m from the beginning of the line) and at node 91 (distance on the trunk cable 8 m from the beginning of the line). In general, such an arrangement will result in a correct operation of the system.



Line Reflections Caused by Stub Lines (15022)

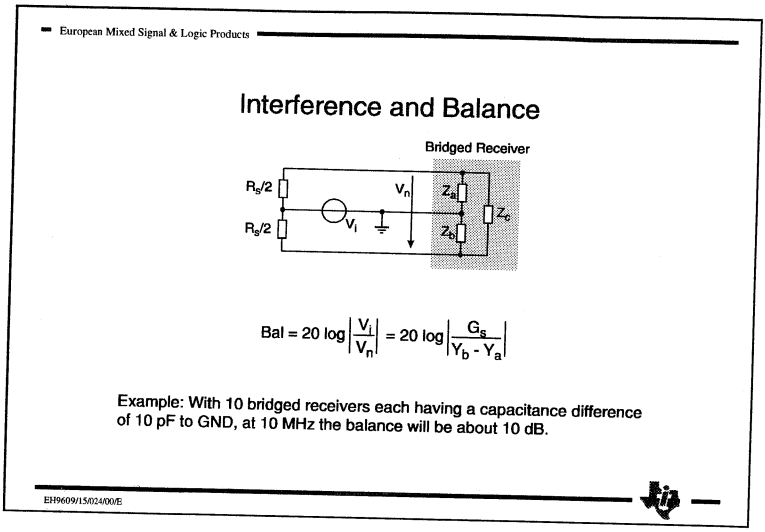
With a stub line length of 0.5 m the line reflections become already evident. (Note that each end of the various stub line generates no line reflections). The sum of these reflections leads to an increase of signal distortion with increasing distance form the generator. The three signals shown are taken at node 11 (generator output), node 51 (distance on the trunk cable 4 m from the beginning of the line) and at node 91 (distance on the trunk cable 8 m from the beginning of the line). Even if the distortion is already measurable, reliable operation of the interface should be possible.

Note: The standard ISO 8482 recommends a maximum stub line length of 5 m.



Line Reflections Caused by Stub Lines (15023)

When increasing the stub line length up to 5 m the signal distortions become severe. The three signals shown again taken at node 11, node 51, and at node 91. Under these circumstances reliable operation of the interface can no longer be guaranteed.

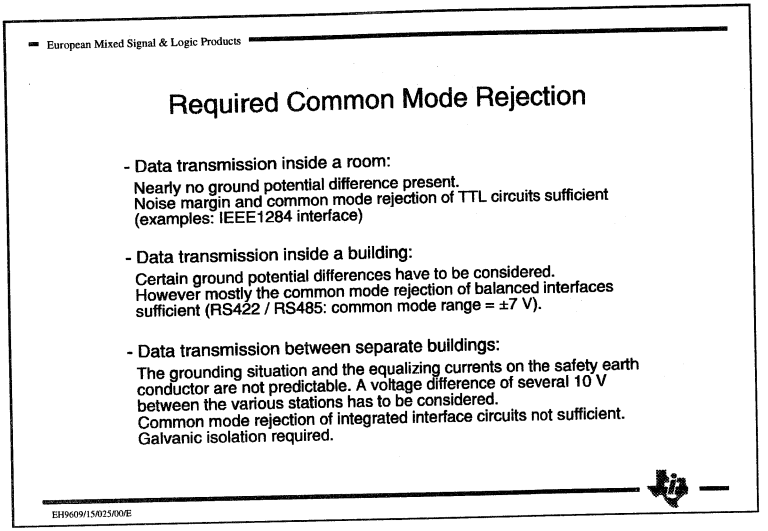


Interference and Balance (15024)

As long as the input impedance of both inputs of a balanced transceiver are equal, the interface becomes balanced bridge circuit, where the common mode voltage V_i will not cause any voltage difference between to two inputs of a receiver. When however due to stray capacitances of the connector or of the printed circuit board the input capacitance of the two receiver inputs becomes different, the bridge circuit becomes unbalanced. In the above picture for low frequencies R_s is the output impedance of the generator and for high frequencies the line impedance. Z_a, Z_b, and Z_c are the impedances of the receiver(s). With a few simplifications one can calculate the balance of the bridged receiver(s):

$$Bal = 20\log\left|\frac{V_j}{V_n}\right| = 20\log\left|\frac{G_s}{Y_b - Y_a}\right|$$

With a line impedance Z_o = 120 Ω and 10 bridged receivers each having a capacitance difference of 10 pF to ground, at 10 MHz the balance would be about 10 dB. At a frequency of 50 MHz, the configuration would appear to have one conductor grounded.



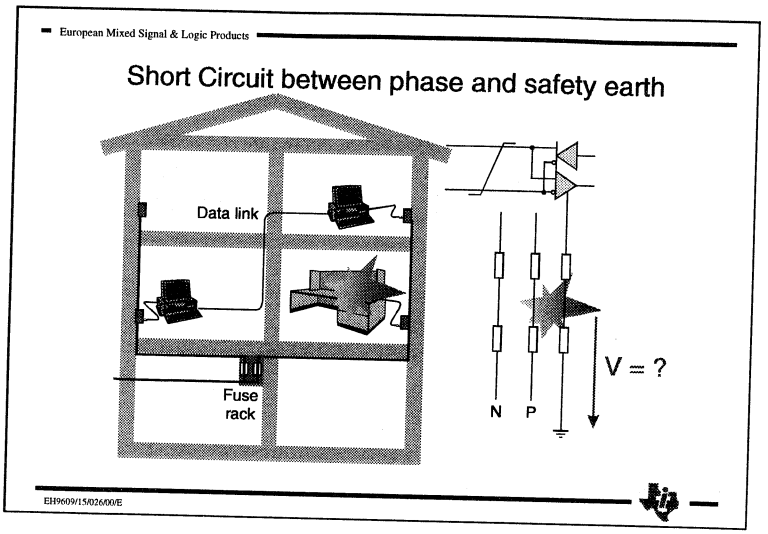
Required Common Mode Rejection (15025)

Depending on the environment where the interface has to operate, the requirements of common mode rejection are vary.

If the interface has to operate in a single room - e.g. a laboratory - nearly no common mode rejection is required. All generators and receivers are connected to the protection earth reference point of this room. The voltage difference on the ground lines in practise is zero. In such an environment the performance of simple TTL type interfaces (IEEE 488, IEEE 1284) is fully sufficient as the widespread problem-free application of these circuits proves.

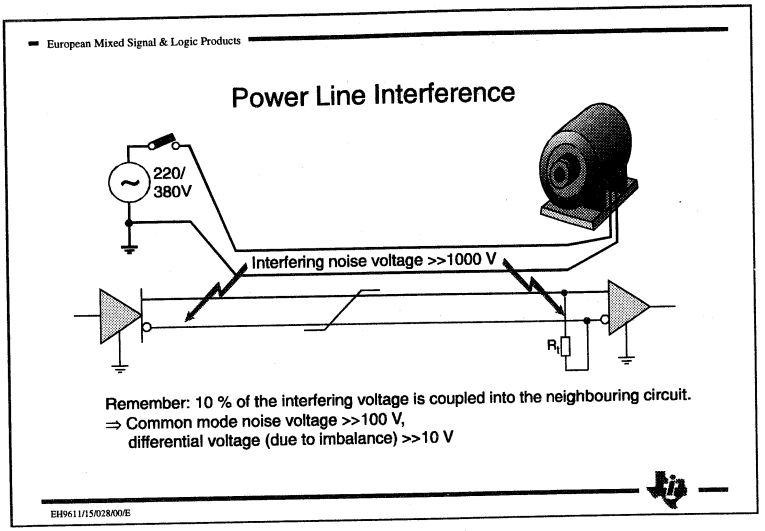
If the netwok is distributed over a building, some common mode rejection is required. In many applications the common mode rejection of integrated balanced interface circuits ($V_{cmmax} = \pm 7$ V) may be sufficient. If however larger energy consuming equipment is located in the building (e.g. motors for lifts or fans air conditioning) a ground potential shift of by far more than 7 V has to be considered. Please note that e.g. safety regulations in Germany allow a ground potential difference of up to 50 V in a building.

If the network is distributed over several buildings, nearly no predictions can be made concerning the ground potential difference. One should not use simply a balanced interface with an integrated interface circuit (e.g. SN75176) alone. The common mode rejection is inadequate. Further measures like galvanic isolation are essential.



Short Circuit between Phase and Safety Earth (15026)

A simple example illustrates the possible causes for the destruction of an interface and the need for galvanic isolation. And both ends of a building two personal computers are located. The computer are connected to each other via an interface. These equipment's are supplied via separate rising mains. By accident a short circuit happens between the phase and the protective earth conductor at one end of building. The resulting short circuit current in the protective earth conductor will lead to rise of the ground potential in this area by several 10 V. This rise of voltage becomes now the common mode voltage in the interface between the two computers. Before the fuse is blown the interface will be destroyed.



Power Line Interference (15028)

A network has been installed in building. By accident some time later a power line is placed adjacent to the network cable. When the load on this power line (e.g. an electric motor) is turned on or off, due to the switch bounce we expect a high noise voltage of up to several thousand volts. About 10 % of this voltage is coupled into the interface as a common mode voltage. The pulse width of this interference will be twice the propagation time of the wave in the interface. The source impedance of this interference is the line impedance of the interface (about 100 Ω). Therefore the common mode interference in the interface will be up to several 100 V. The differential voltage in the interface will be several 10 V. Both values are far above the limits of integrated circuits. The final result will be an immediate destruction of the interface due to both, with excessive common mode voltage as well as and excessive differential voltage.

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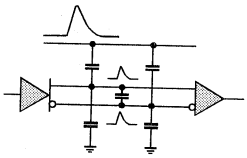
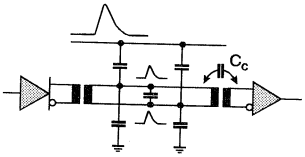
Why Galvanic Isolation?



Common mode noise is coupled into the balanced interface. This leads to a very high voltage at the integrated circuit's terminals.



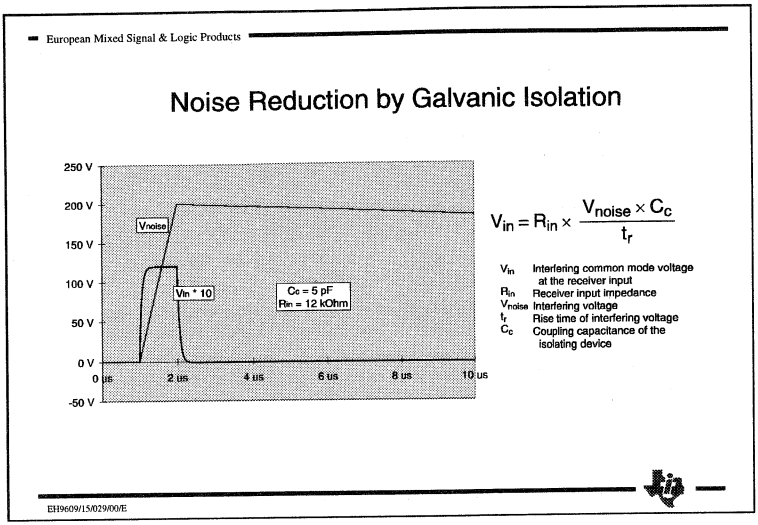
A galvanic isolation rejects most of the interfering noise. Therefore this arrangement is applicable even in a very noisy environment.
Take care of a low transformer coupling capacitance C_C.

Note: 10 % of the amplitude of the interfering signal is coupled into to the circuit.

EH9609/15027/00/E

Why Galvanic Isolation (15027)

Owing to interference caused by the various noise sources in the neighbourhood of an interface, one must consider common mode noise in the order of several 10 to 100 volts and differential noise in the order of some 10 volts. This interference in any case can destroy the integrated circuits in the interface. The only way to harden the interface is galvanic isolation. Such a circuit isolates the integrated circuits from the common mode noise. By using a careful circuit arrangement which also takes care of the balance of the interface the differential noise voltage can be lowered. When selecting the components for galvanic isolation the designer has to take care of a low coupling capacitance between the input and output of the isolating circuit.



Noise Reduction by Galvanic Isolation (1529)

Due to the coupling capacitance between the input and the output of the isolating component some noise is still coupled in to the secondary circuit. In the example discussed here the following assumptions are made:

- Coupling capacitance of the transformer used for isolation C_c = 5 pF.

- Input impedance of the integrated circuit at the secondary side of the transformer R_{in} = 12 kΩ.

- Common mode noise voltage in the balanced cable V_{noise} = 200 V.

- Rise time of the common mode noise voltage t_r = 1 µs. Owing to the large inductance of the interference coupling path, the rise time of the noise is mostly not very high.

The noise voltage at the input of the integrated circuit can be calculated by the formula:

$$V_{in} = R_{in} \frac{V_{noise} \cdot C_c}{t_r} = 12k\Omega \frac{200V \cdot 5pF}{1\mu s} = 12V$$

The resulting noise voltage may still be too high for a correct operation of the interface (V_{cmmax} = ± 7 V at ISO 8482). But due to the low coupling capacitance and the resulting high impedance of the coupling path, destruction of the integrated circuit by the interfering noise can be avoided.

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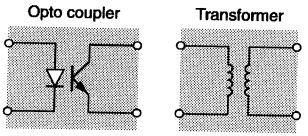
Galvanic Isolation

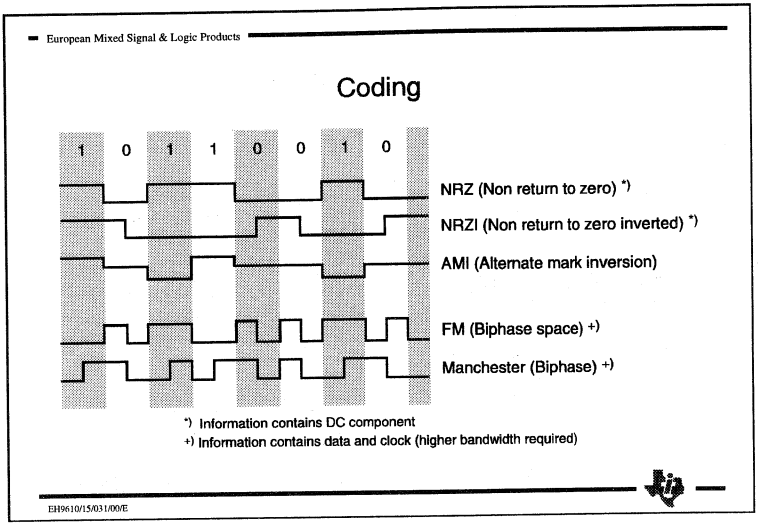


	Opto coupler	Transformer	Remarks
Maximum data rate	>10 MBit/s	>10 MBit/s	Limiting factor: line length
Common mode rejection	fair	good	Coupling capacitance
TTL compatibility	yes	no	
Transfer of signals with DC content	yes	no	Start-stop operation (UART)
Bi-directional transmission	no	yes	Bus applications
Isolation voltage	>1000 V	>1000 V	Safety regulations

EH9609/15030/00/E

Galvanic Isolation (15030)

Two components are often used for a galvanic isolation in an interface: the optocoupler and the transformer. The pros and cons will be shortly discussed. In terms of maximum data rate there is no big difference. It is easy to transfer via a small ring core transformer 10 MBit/s and more. The same performance can be achieved also by using an optocoupler. The limiting factor are mostly the losses of the transmission line. The common mode rejection is at least fair for both components. The transformer may have some advantages due to a truly balanced circuit possible with this component. TTL compatibility is a major advantage of an optocoupler in terms of circuit simplicity and cost. The optocoupler can also transmit information containing DC, which allows the use of Universal Asynchronous Receivers and Transmitters (UART). A transformer on the other hand is capable of transmitting data bi-directionally, which results in a lower cost in this kind of application. The isolation voltage is sufficient with both components. The isolation voltage required to handle the common mode noise even under difficult situations is in the order of 500 V. Some legal regulation may require an isolation voltage of up 2000 V, which can also be achieved with both types of circuits easily.



Coding (15031)

When transmitting data the information has to be presented - say coded - in a way which allows easy recovery of the data at the receivers - where easy recovery may have a different meaning depending on the requirements of the application.

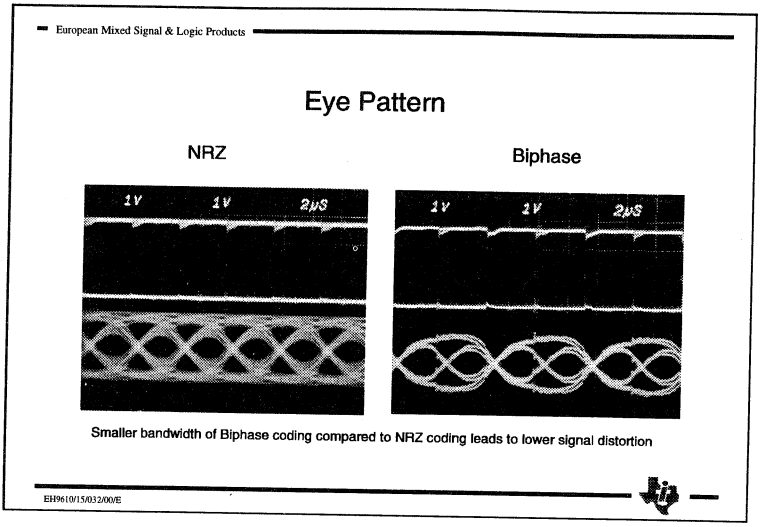
The simplest coding scheme is NRZ (Non Return to Zero). The information is presented as a sequence of the bits to be transmitted - highs and lows, ones and zeros, or marks and spaces. The transition from one state to the opposite state occurs at the boundaries of the bit interval.

A coding scheme which reduces the number of transitions, and by this the energy required, is NRZI (Non Return to Zero Inverted. A transition takes place in the centre of the bit interval (alternating from high to low or from low to high) whenever a zero ('0') in transmitted. During the transmission of ones ('1') the state is not changed.

AMI (Alternate Mark Inversion) coding uses three states. When a zero is transmitted the status of the line is zero. A one is represented by alternating positive or a negative voltage intervals. Unlike the previous coding schemes, AMI coding contains no DC components and can therefore be used for inductive and capacitive coupling.

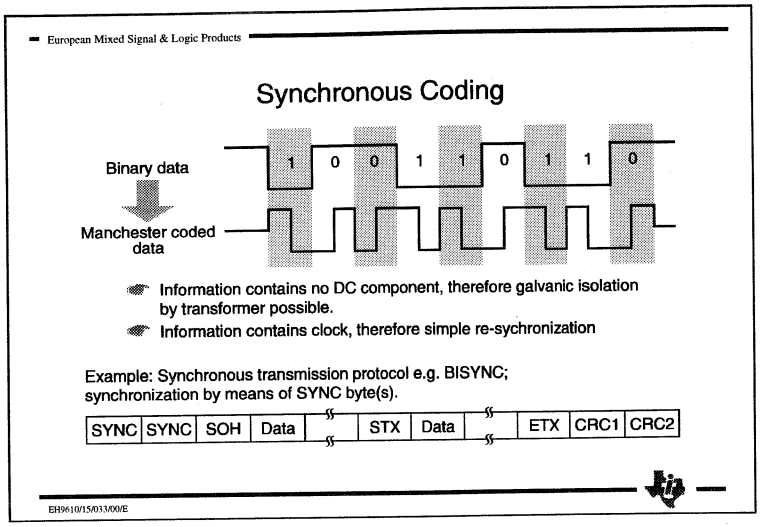
In the Biphase Space coding scheme, a one is represented by a transition at the bit boundaries and no transition during the bit interval, while a zero is represented by an additional transition in the middle of the bit interval. The transitions at the bit boundaries allow a simple clock recovery. The information transmitted contains no DC component.

Manchester coded data show a transition at the middle of each bit interval: A positive transition when a one is transmitted, a negative transition when a zero is transmitted. Further transitions at the bit boundaries occur at successive ones or zeros. The mid-bit transitions convey inherent timing information and allows a simple clock recovery. The information transmitted contains no DC component.



Eye Pattern (15032)

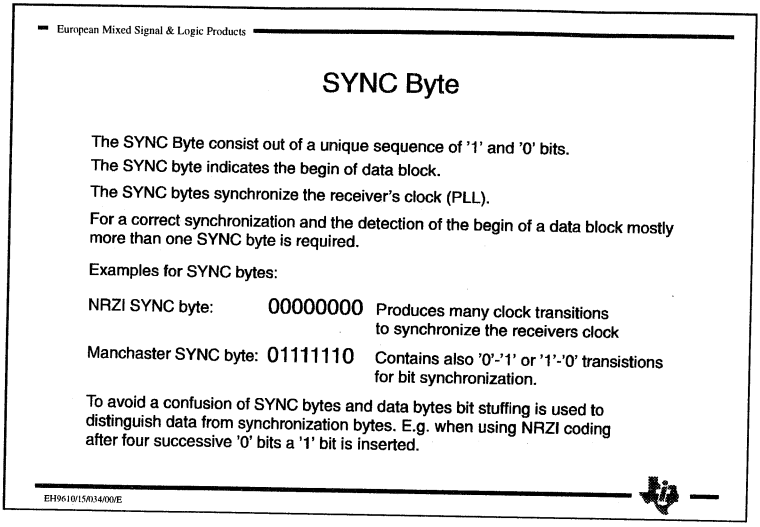
Using NRZ encoding, the frequency bandwidth of the data transmitted depends on the random sequence of the ones and zero of the data. The highest frequency is determined by half the data rate. The lowest frequency is determined by the longest sequence of successive ones or zeros. Biphase encoding reduces the required bandwidth. The highest frequency is determined by the clock frequency, the lowest frequency by half the data rate (= 50 % of the clock rate). This fact reduces the noise and simplifies data recovery.



Synchronous Coding (15033)

For easy data recovery synchronous encoding is used. Beside the data the information transmitted contains also the clock which allows a simple regeneration of the clock signal at the receiver. An encoding scheme containing no DC content like Manchester encoding allows cost effective galvanic isolation via transformers.

A protocol, the Binary Synchronous Communication Protocol (BISYNC), controls the data transfer. The beginning of the control character SOH indicates the beginning of an optional header. The control character STX indicates the beginning of the data to be transmitted. The data block is terminated by the control character ETX, which also indicates the following block check character(s). The message is headed by SYNC bytes which allow the re-synchronisation of the clock at the receiver.

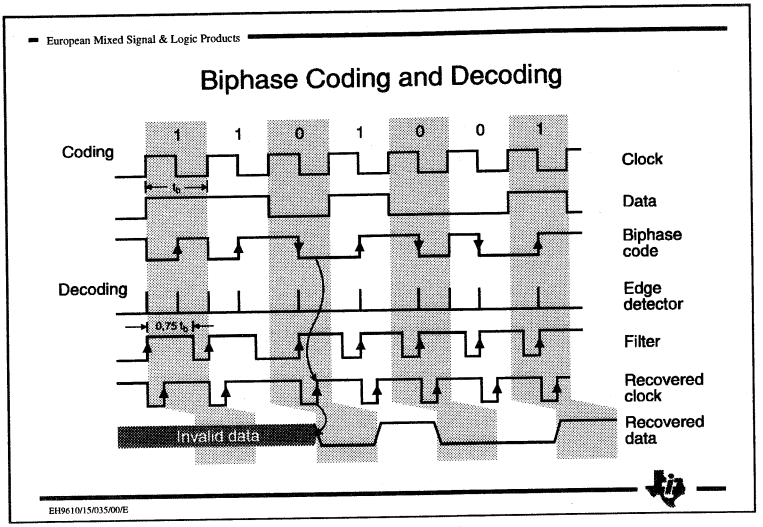


SYNC Byte (15034)

The SYNC byte indicates the beginning of a transmission. This byte consists of a unique sequence of ones and zeros to differentiate this byte from the following control and data bytes. The SYNC byte is used to synchronise the receiver's clock. For a correct synchronisation often several SYNC bytes in sequence have to be transmitted.

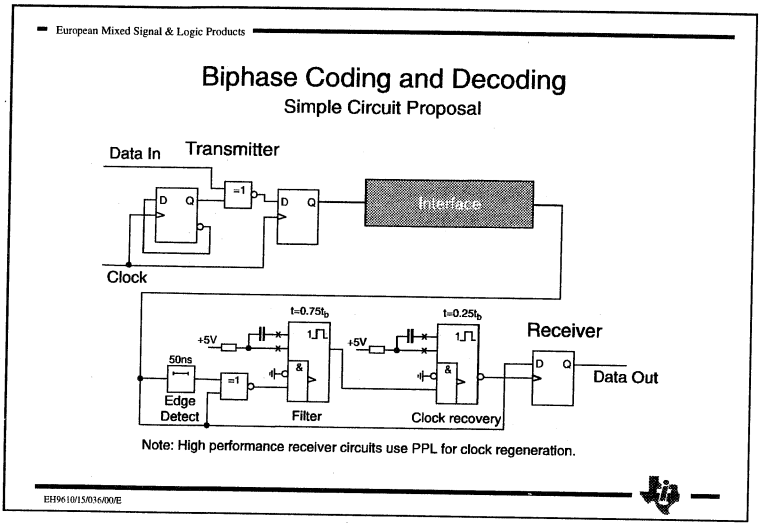
For a fast synchronisation this byte has to generate many clock transitions. Therefore the structure of the SYNC byte depends on the encoding scheme used. NRZI encoding for example generates a transition by successive zeros. Because of this in this application a SYNC byte may consist of eight successive zeros. When using Manchester encoding the synchronisation of the receiver requires 0-1 or 1-0 transitions. Therefore an appropriate SYNC byte may be '0111 1110'.

To avoid confusion between the SYNC byte(s) and the following data in case of a data byte with the same content as the SYNC byte, bit stuffing is used. When using NRZI encoding, after four successive zeros in the bit stream a one bit is inserted. The receiver logic later on removes these stuff bits to regenerate the original data.



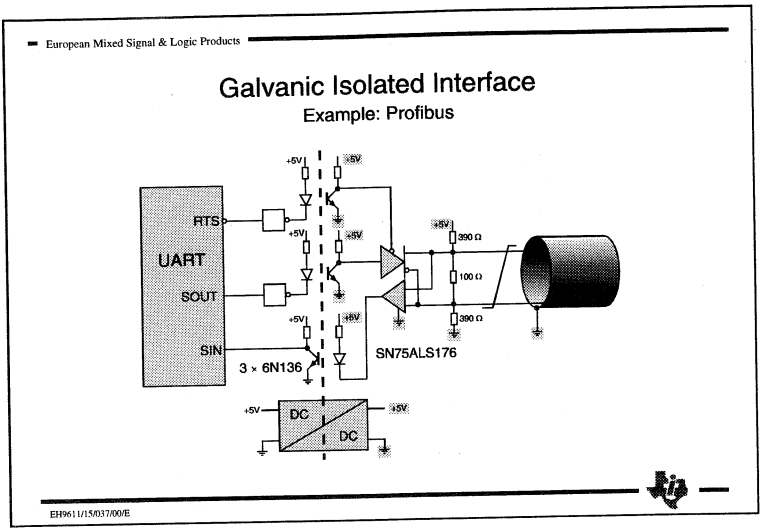
Biphase Encoding and Decoding (15035)

When using Manchester encoding the encoder consists of an exclusive-OR gate only which combines clock and data. The decoding circuit is a little bit more complex. An edge detector generates a short trigger pulse at every positive and negative transition. These pulses trigger a monostable multivibrator which generates pulses with a duration of 75 % of the bit interval. After the first 1-0 or 0-1 transition in the data stream this circuit is synchronised to the original transmitter clock. A second monostable multivibrator with a pulse width of 25 % of the bit interval is used to sample the data, e.g. to clock the data into a flip-flop. At the output of this flip-flop the decoded data are available again.



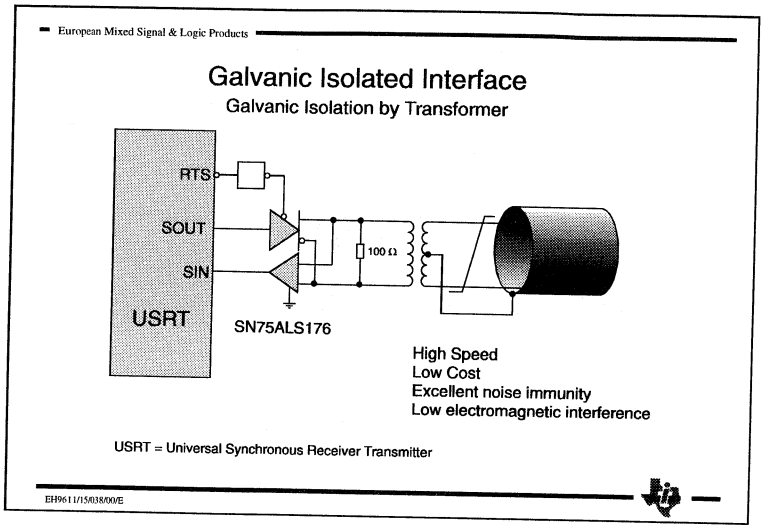
Biphase Encoding and Decoding (15036)

The picture above shows the circuit diagram of a Biphase encoder and decoder. For an exact duty cycle of 50 % of the transmitter clock, this clock is generated by a 2:1 divider from a clock of twice the frequency. A further flip-flop following the exclusive-OR gate prevents spikes in the encoded data. These may be caused by a phase shift between the transmit clock and the data. The interface consists of an appropriate circuit e.g. a balanced interface according to ITU-U V.11 (= EIA-RS422). The transition detector at the receiver is made by a delay line (t_d = 50 ns) and an exclusive-OR gate. This circuit triggers the filter monostable multivibrator. The output of the later circuit triggers the second monostable multivibrator which triggers the D flip-flop. At the output of this flip-flop the data can be obtained.



Galvanic Isolated Interface (15037)

A galvanic isolated interface, as may be used in a Profibus application, is shown in the above picture. The transceiver is built up be using a SN75ALS176. The resistor network at the output of this circuit, terminating the transmission line, provides the biasing of the circuits in case of inactive transmitters. The shield of the cable is connected to the GND terminal of this interface circuit. The galvanic isolation of the transmit data, the receive data, and the direction control is done via optocouplers. The designer has to select the optocouplers according to the maximum data rate of the interface. The optocoupler 6N136 allows a data rate of up to 1 MBit/s. The controller is an Asynchronous Receiver and Transmitter (UART), which is integrated in many of today's microprocessors. A DC-DC converter is required to provide the supply voltage to the transceiver. This circuit is probably the most expensive part of the interface, which may offset the cost advantage of an asynchronous transmission protocol.

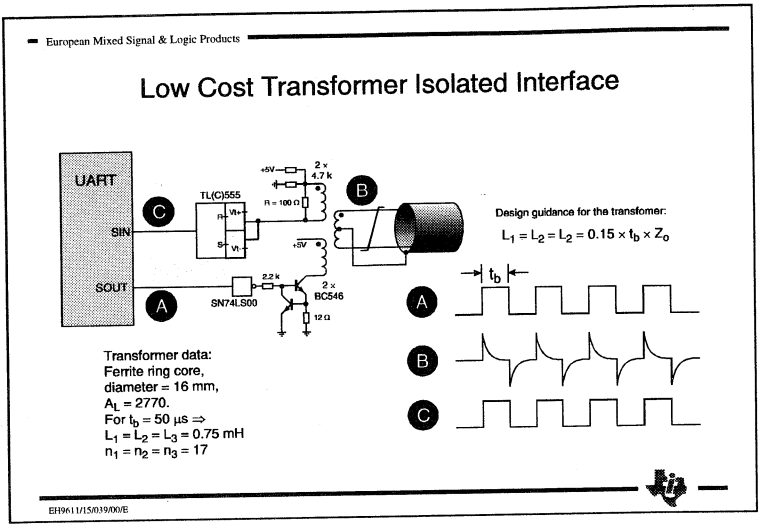


Galvanic Isolated Interface (15038)

By using a transformer isolated interface, the number of components, and thus the cost of the interface, can be reduced considerably. The expensive DC-DC converter is no longer required. The transceiver circuit is again a SN75ALS176 or a similar component. The transformer is made by simple ring core with two windings. The secondary winding may have a tap at the centre to connect the shield of the cable. With a line impedance Z_o and a bit duration t_b the inductance L of the windings is calculated as follows:

$$L = 5...10 \cdot Z_o \cdot t_b$$

Such an arrangement provides the lowest coupling capacitance between the line and the system and therefore the best common mode rejection. The disadvantage of this circuit concept is the need of a Universal Synchronous Receiver and Transmitter (USRT), which is more expensive than an UART. However this disadvantage is mostly offset by the fact that the USRT contains all the control logic required to handle more complex protocols. The USRT for example generates the SYNC byte(s) as well as the error check bytes and handles the synchronisation of the receiver as well error checking.

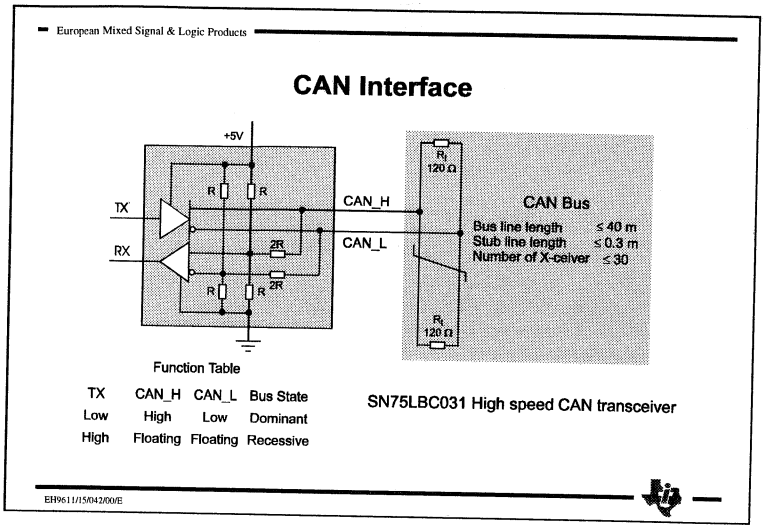


Low Cost Transformer Isolated Interface (15038)

In the picture above, is a simple transformer isolated interface which uses as a controller a low cost UART. The line driver consists of a current source built up by two bipolar transistors BC546. Controlled by the serial output of the UART this current source forces a current of about 60 mA into the transformer. This current is differentiated, so that one gets a positive voltage spikes on the secondary winding of the transformer when the current is turned on and a negative voltage spike when current is turned off. During a bit interval the differentiated voltage has to decrease to about 0 V again. For a correct operation of this circuit the inductance L of the windings of the transformer has to be calculated as follows:

$$L_1 = L_2 = L_3 = 0.2 \cdot Z_o \cdot t_b$$

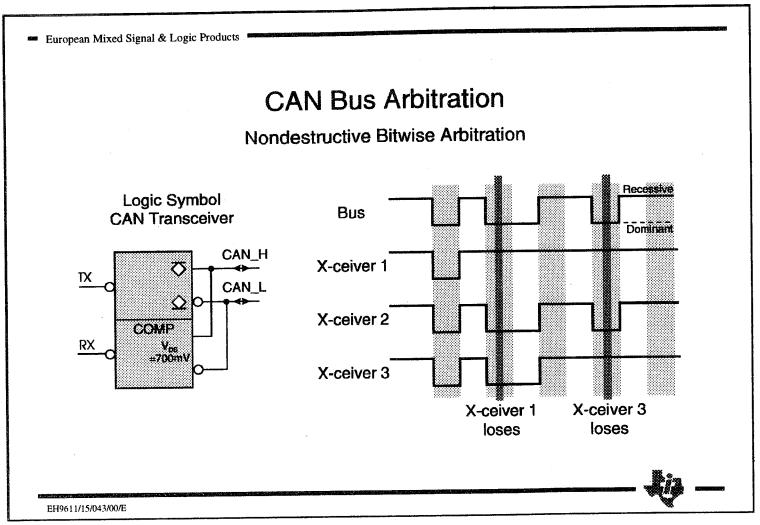
At the line end the alternating positive and negative voltage spikes have to be reassembled again to the original sequence of ones and zeros. This is done easily by a Schmitt trigger, which is biased by a voltage equal to the middle between the positive and the negative threshold voltage of the Schmitt trigger. The Schmitt trigger in this application is built from the well known timer circuit TLC555. By shorting together the Threshold and Trigger input of this circuit, one gets a Schmitt trigger with threshold voltage at 1/3 and 2/3 of V_{cc}.



CAN Interface (15042)

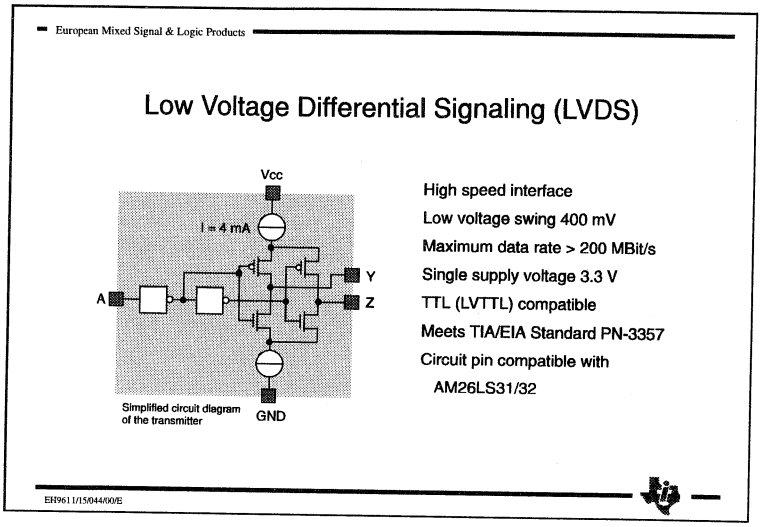
The Controller Area Network has been developed for automotive applications to replace the complex cable in cars by a two wire interface. The architecture of the interface is similar to the balanced interfaces described before with some modifications required by automotive applications. The line length is limited to 40 m, which is sufficient for the intended application. Up to 30 transceivers may connected to the bus with a stub line length of up to 30 cm. The line has to be terminated at both ends by termination resistors of 120 Ω. To handle fast arbitration between various bus members in the car, a different circuit is found at the transmitter output. One output called CAN_H is an open collector pull-up circuit, while the complementary output CAN_L is an open collector pull-down output. A low level at the TX input forces both outputs into the active state (dominant state), while a high level at this input turns off both output transistors (recessive state). The function of a CAN transmitter can be emulated by a standard balanced interface circuit like the SN75176, when connecting the D input to high and by using the output enable input DE as the TX input. The line output terminals of the interface circuit are designed to withstand the high noise in a ca environment. The terminals CAN_H and CAN_L may be shorted continuously to a voltage between -2 V and +20 V. The differential amplifier at the receiver input has a intentionally built-in offset voltage V_{TD} = 900 mV. This feature forces the receiver output RX to the high state when the inputs are left open if the recessive state is present on the bus.

The original intention has been a multi-point interface where all transceivers where connected along one bus. This arrangement is called High Speed CAN and allows a data rate up to 1 MBit/s.



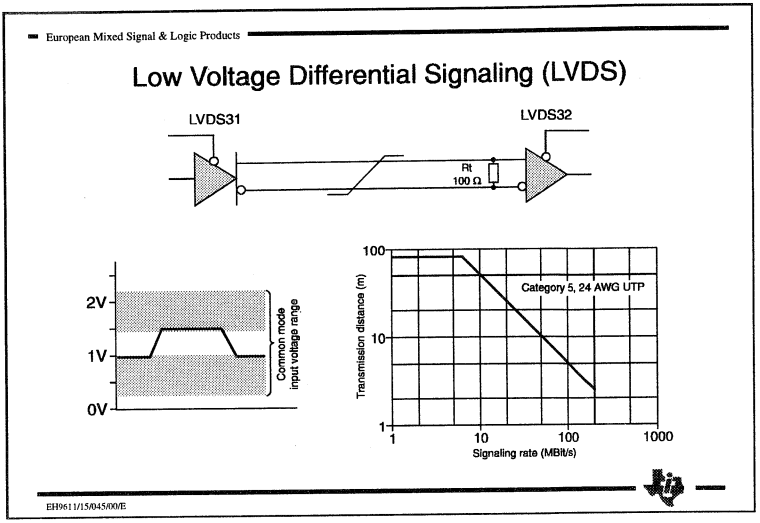
CAN Bus Arbitration (15043)

The many modules to be attached to the Controller Area Network require a fair arbitration scheme where no bus member will be put in a disadvantage. This feature is accomplished by the circuit of the transceiver outputs and the bus protocol. Whenever a module tries to access the bus the first part of the message transmitted is a start bit followed 12 bit containing the arbitration field, which includes the priority of the module. Due to the dominant (high) and recessive (low) logic states generated by the transmitter, the dominant state transmitted governs the recessive state and forces the bus to the high state. The example above shows the simultaneous access to bus of three transceivers. All three transceivers apply the start bit (dominant state) to the bus at the same time to indicate the demand for the bus. The next bit transmitted by all modules (first bit of the arbitration field) is low (recessive state). Therefore the bus becomes low. During the third bit interval the transceivers 2 and 3 output the dominant state, transceiver 1 the recessive state. The result is a high state on the bus. The recessive state of transceivers 1 is over-written and due to this fact this module turns itself into listener state again. The remaining modules continue to get the right over the bus. With an arbitration field length of 12 bits in theory up to 4096 modules can request the bus simultaneously, while the decision for the access of the modules with the highest priority is made during a few microseconds only.



Low Voltage Differential Signalling - LVDS (15044)

The increasing demand for high speed applications requires a new circuit approach. The limiting factor of the established interfaces like ITU-T V.11 (EIA-RS 422) is the high voltage swing of about 3 V, which causes a high power dissipation. Therefore in a high speed environment it is advantageous to reduce the voltage swing. The proposed standard TIA/EIA PN-3357 recommends a voltage swing of 400 mV only. This improvement in combination with an advanced semiconductor technology allows a data rate of up to 200 MBit/s. The transmitter output circuit is realised by a current source providing an output current of 4 mA. A differential switch forces the current in either the positive or the negative direction into the line. With a line impedance Z_o = 100 Ω and a corresponding termination resistor the voltage swing on the transmission line will be 400 mV. The receiver contains a differential amplifier which guarantees a good common mode rejection. The common mode input voltage range of the receiver is V_{cm} = 0.225...2.175 V.



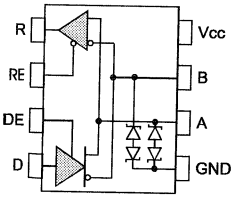
Low Voltage Differential Signalling - LVDS (15045)

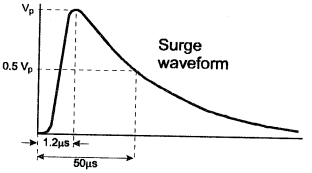
The maximum data rate in a LVDS interface depends on the cable quality and the line length. As already mentioned at high frequencies the skin effect leads to considerable losses on the transmission line. Therefore for a high data rate the user has to choose a cable with low losses. To achieve a data rate of 200 MBit/s category 5 unshielded twisted pair cable is recommended. This type of cable allows a line length of about 2 m at this speed. With reduced data rate the line length can be increased up to about 100 m. Longer transmission lines are not recommended owing to the limited common mode range of the receiver and the larger common mode noise to be expected of long transmission length.

European Mixed Signal & Logic Products

Interface Circuit for Rough Environmental Conditions

SN75LBC184 - Thunderball





Integrated transient voltages suppression to 500W peak

ESD protection Human Body Model 15 kV
Machine Model 600 V

Controlled driver output slew rate ($t_r/t_f \approx 1$ µs) allows longer unterminated lines and longer stub lines with data rates up to 250 kBit/s

1/2 Unit Load allows 64 transceivers connected on bus

Interface Circuit for Rough Environmental Conditions (15046)

To simplify the application of interface circuits in a rough environment the SN75LBC184 includes additional protection measures to withstand surges up to 500 W_{peak}. Furtheremore the circuit withstands an electrostatic discharge of 15 kV (Human Body Model) and 600 V (Machine Model). The LinBiCMOS process provides a very low shutdown supply current I_{cc} = 250 µA. An increased input impedance reduces the load to 0.5 UL only, which allows up to 64 transceivers connected to a bus. For easier implementations the output slew rate has been slowed down to t_r/t_f ≈1 µs. This feature allows a longer unterminated line and longer stub lines.

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RS-485 Data Transmission Circuits

Device	Devices	Device	Key
Line Drivers	4	SN7172	Industry Standard
		SN7174	Industry Standard
		SN75ALS172	High Speed
		SN75ALS174	High Speed
		SN75LBC172	High Speed / Low Power
		SN75LBC174	High Speed / Low Power
Line Receivers	4	SN7173	Industry Standard
		SN7175	Industry Standard
		SN75ALS173	High Speed
		SN75ALS175	High Speed
		SN75LBC173	High Speed / Low Power
		SN75LBC175	High speed / Low Power
Line Transceivers (Drivers/ Receivers)	1	SN75176A	Bidirect Xver -like
		SN75176B	Industry Standard
		SN75177B	Industry standard bipolar
		SN75178B	Industry standard bipolar
		SN75ALS176	High Speed
		SN75ALS176A	Very High Speed
		SN75ALS176B	Ultra High Speed
		SN75LBC176	Ultra Low Power
	1/1	SN75179B	Industry Standard
		SN75LBC179	High Speed / Low Power
		SN75ALS180	Full Duplex Communication
		SN75LBC180	High Speed / Low Power
		SN75ALS181	Full Duplex Communicatio
	2/2	SN75177	High Speed
		SN75178	High Speed
		SN75ALS177	High Speed
		SN75ALS178	High Speed
		SN75ALS179A	High Speed
	3/3	SN75ALS181A	High Speed
		SN75ALS177I	High Speed
	9/9	SN75976A/76Z	Low Power/High Speed
		SN75LBC978	Low Power with WRAP
		SN75LBC968	Industry Accpt Termination

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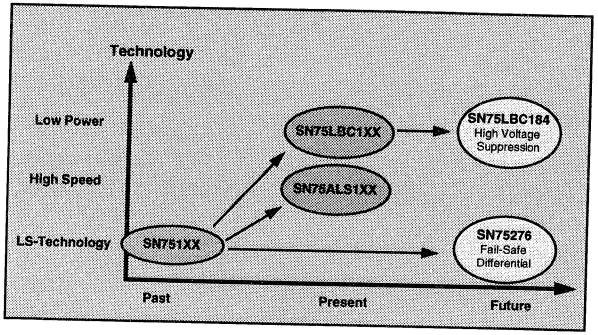
RS-485 Roadmap



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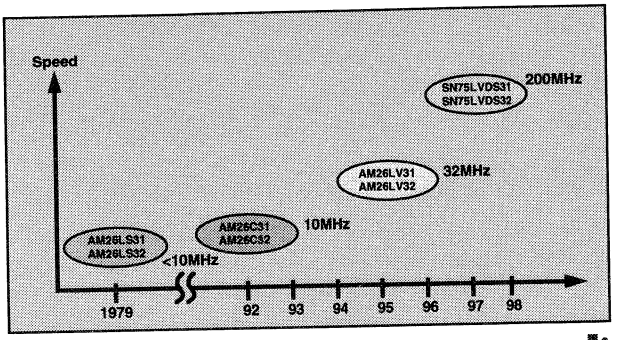
High-Speed Quad Differential Line Driver/Receiver
RS-422 Roadmap



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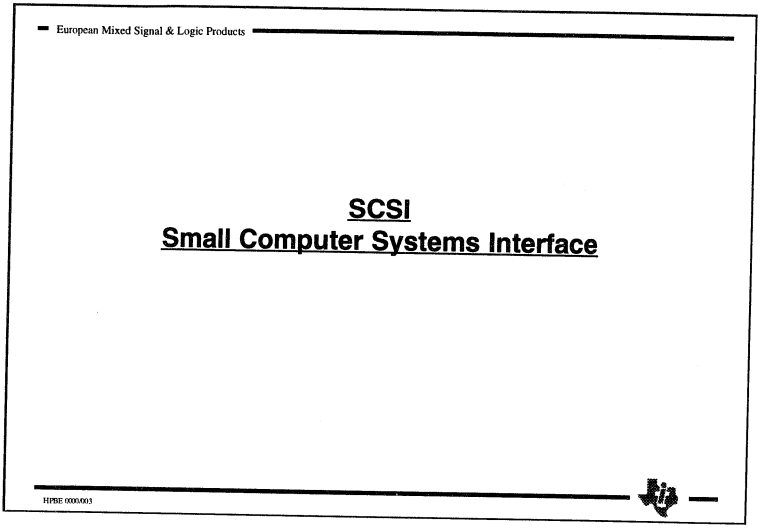
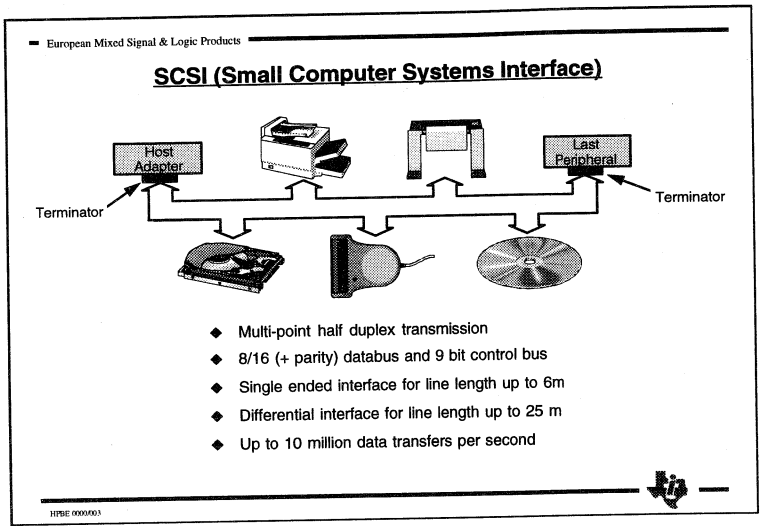
ADVANCED HIGH-SPEED INTERFACES

HPBE 0000/003


European Mixed Signal & Logic Products
SCSI
Small Computer Systems Interface
HPBE 000/003



SCSI Overview

Small Computer System Interface (SCSI) details the ANSI specification for a peripheral bus and command set. The specification defines a high-performance peripheral interface that distributes data independently of its host, helping to free up the host for more user-oriented commands or activities. There are a large number of disk drives, notebooks, PCs, and CD-ROM drives which incorporate a SCSI port.

SCSI Physical Layer

There are two electrical specifications referred to in the SCSI standard - single ended and differential SCSI.

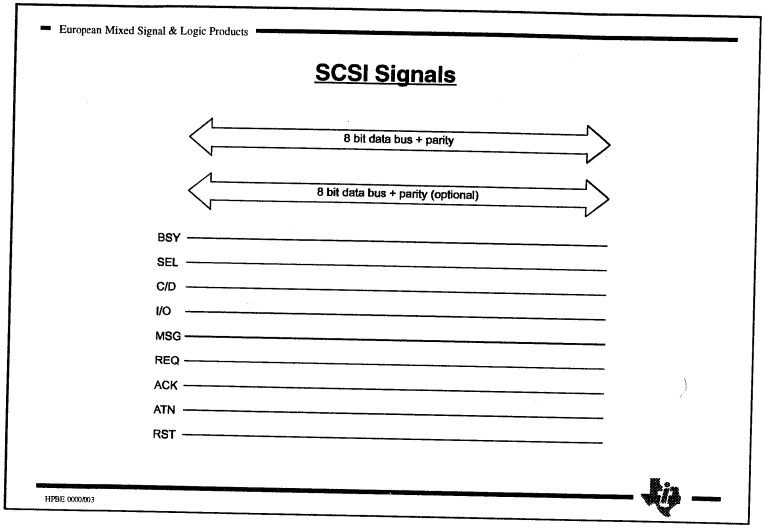
It is beyond the scope of this section to discuss the complete SCSI standard, we shall concern ourselves here with the physical layer only. For more information on the standard you are encouraged to refer to the numerous publications on SCSI.

Single-Ended Interface

The single-ended driver and receiver configuration utilizes TTL logic levels and is primarily intended for applications with a cabinet, the maximum line length being limited to 6 meters and the data rate is normally limited to 5 million transfers per second (Mxfers/s), although careful system design can create a maximum transfer rate up to 10 Mxfres/s.

Differential Interface

The differential driver and receiver configuration uses the RS-485 standard and is primarily concerned with transmitting data between cabinets, on heavily loaded buses, or in high-reliability systems with a maximum line length of 25 meters and data rates up to 10 Mxfers/s.



The SCSI Signals

Basic SCSI is an eight bit (plus parity) parallel I/O bus with nine control/handshaking lines, making 18 lines in total. More recently, to increase the data throughput, the standard has made provision for the data bus to be extended to 16 bits whilst maintaining the nine control lines. This is referred to as wide SCSI. A brief description of the signals follows now.

DB0 - DB7, DB(P):

Eight data-bit signals, plus a parity-bit signal that form a DATA BUS. DB(7) is the most significant bit and has the highest priority during the ARBITRATION phase. Bit number, significance, and priority decrease downward to DB(0). A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. Data parity DB(P) shall be odd. Parity is undefined during the ARBITRATION phase.

BSY (Busy):

An OR-tied signal that indicates that the bus is being used.

SEL (Select):

An OR-tied signal (has been defined as OR-tied in SCSI-2) used by an initiator to select a target or by a target to reselect an initiator.

C/D (Control/Data):

A signal driven by a target that indicates whether CONTROL or DATA information is on the DATA BUS.

I/O (Input/Output):

A signal driven by a target that controls the direction of data movement on the DATA BUS with respect to an initiator. True indicates input to the initiator. This signal is also used to distinguish between SELECTION and RESELECTION phases.

MSG (Message):

A signal driven by a target during the MESSAGE phase.

REQ (Request):

A signal driven by a target to indicate a request for an ACK information handshake.

ACK (Acknowledge):

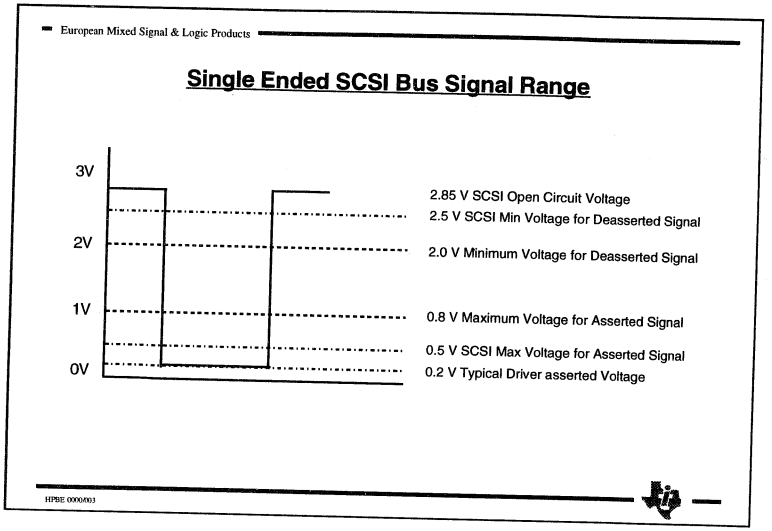
A signal driven by an initiator to indicate an acknowledgement for a REQ information transfer handshake.

ATN (Attention):

A signal driven by an initiator to indicate the ATTENTION condition.

RST (Reset):

An OR-tied signal that indicates the RESET condition.



Single Ended SCSI Termination

Termination of the single-ended SCSI bus is becoming increasingly important as designers strive for faster system speeds. If error free data rates of 10 Mbps over a 6-meter bus are to be achieved then signal integrity must be preserved. Termination reduces unfavorable transmission line effects such as reflections and distortin that can degrade system performance as signal speeds increase. Proper termination of bidirectional buses, such as SCSI, require terminators at each end of the cable.

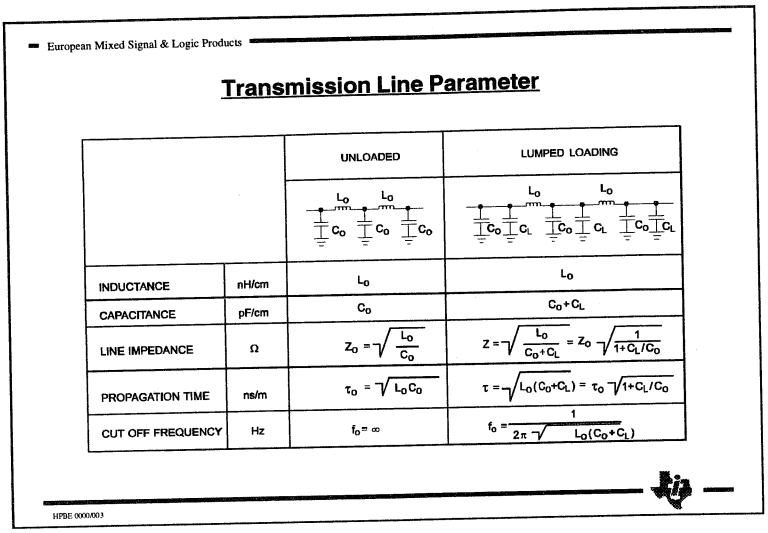
Signal Transitions

The potential for high data rates depends upon quick, clean transition between low and high signal levels.The range of SCSI signals is shown in the figure above. A low to high transition or deassertion of a signal is initiated by an open collector driver switching off and causing an instantaneous voltage step to travel down the line.

The size of the first step depends upon the amount of current in the line (I_L), the characteristic line impedance seen by the signal (Z_0), and the driver low-level output voltage (V_{OL}), and can be calculated as follows:

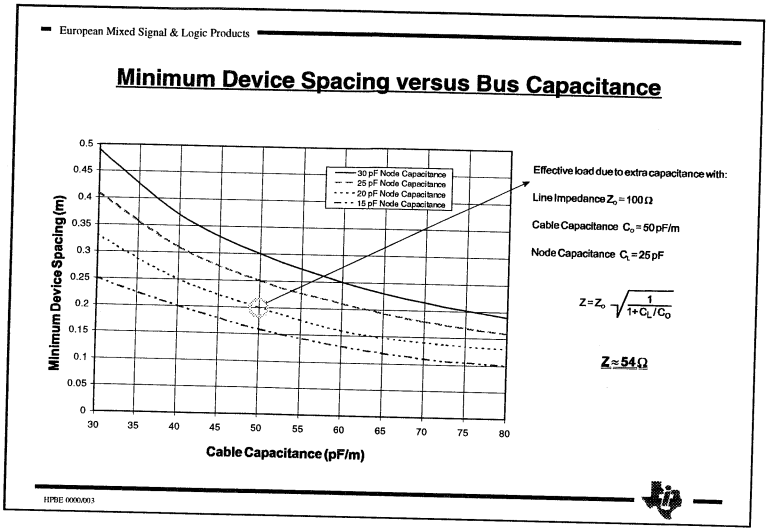
$$V_S = V_{OL} + Z_0 \times I_L$$

To achieve the maximum data rate the first step needs to exceed the receiver threshold voltage in a single transition.



Lumped Loading

Although the impedance of a typical SCSI ribbon cable, which is around 100 Ω, suggests that this requires only limited line-current capability, however the impedance seen by a signal is typically less than the specified cable value. Extra capacitances due to the peripheral connections to the bus reduce the effective load. The figure above shows the equations for the calculation of the effective line impedance, for the unloaded line and the lumped loading. The higher the capacity C_L and the shorter the distance between two bus connections is, the lower becomes the resulting line impedance. The following picture shows a guideline of the maximum device spacing versus the bus capacitance.

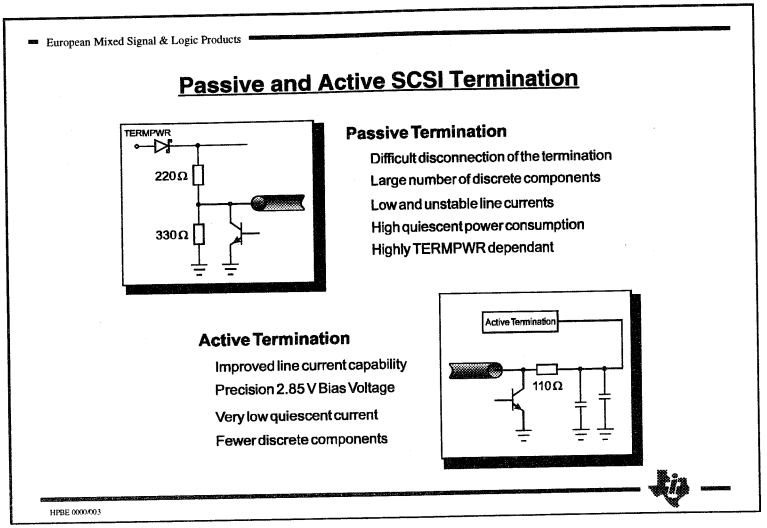


Minimum Device Spacing versus Bus Capacitance

The figure above shows a guideline for the amount of capacitance (and its spacing) that can be added to the Single-ended Fast 20 SCSI bus.

The example next to the picture shows that the original line impedance is reduced from 100 Ω to around 54 Ω, if the Node Capacitance is 20 pF, the Cable Capacitance is 50 pF/m and the minimum device distance is 20 cm.

Therefore it is important to take care of a suitable termination of the SCSI bus. The different terminations are now discussed.



Passive and Active SCSI Termination

SCSI termination has traditionally been carried out using passive termination networks. As illustrated in the figure above these consist of 2 resistors per signal line; a 220 Ω pull up resistor connected to the termination power source (Termpwr), and a 330 Ω pull down resistor connected to ground. The Schotky diode is needed by all termination schemes to protect the power source from reverse currents.

As already mentioned before, the size of the first step can be calculated as follows:

$$V_S = V_{OL} + Z_0 \times I_L$$

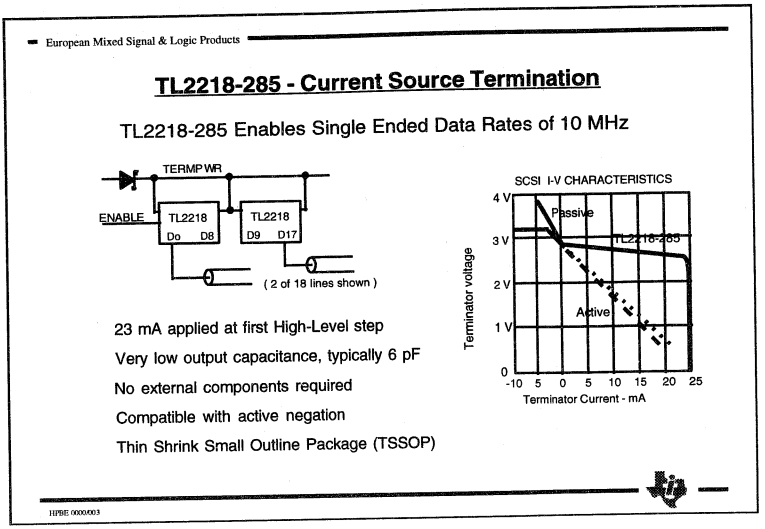
This passive termination typically results in a maximum line current I_L of around 17 mA which can be calculated as follows:

$$I_L = \frac{5V - U_D - V_{OL}}{220\ \Omega}$$

Assuming the terminator is on a capacitively loaded bus, signified by an impedance Z_0 of approximately 75 Ω, then the above equation gives a first step value V_S of 1.8 V - well short of the desired 2.0 V level. In addition to this limited current capability and the power consumption penalty imposed by the resistor dividers, passive terminators also suffer from an unregulated line bias voltage. As a result the line voltage will fluctuate with variations in the load current and Termpwr, leading to smaller noise margins, lower line currents, and reduced data rates.

The most common alternative to passive termination replaces the resistive network with a voltage regulator in series with a single 110 Ω resistor per line. This method, known as Active, Boulay, or Alternative 2 termination, was developed to overcome two of the main shortcomings of passive termination.

The 110 Ω resistors increase the typical line current available on de-assertion to 21 mA. The line current and the high-level noise margins are also more stable since Termpwr is no longer used to set the bias voltage directly. Instead it is used to form the input to the voltage regulator, which then provides a regulated bias voltage.



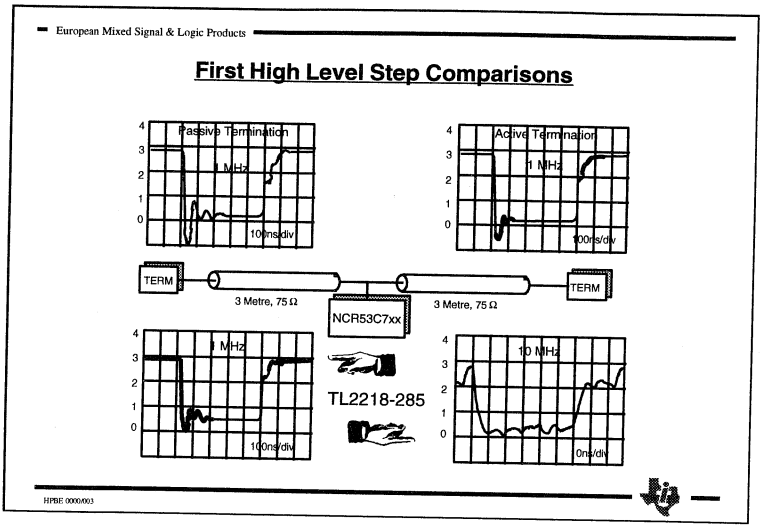
Current Source Termination Using the TL2218

Although active termination brings a number of advantages to SCSI termination these can be further improved upon. The TL2218-285 from Texas Instruments is a completely new type of SCSI terminator which does just that.

The TL2218-285 is a current mode, or non-linear, device which does not contain a voltage regulator. This means that no filtering or stabilizing capacitors are needed, and so unlike 'completely integrated' active terminators, the TL2218-285 needs no external components and it is therefore easy to disconnect the terminator.

Another major difference between the TL2218-285 and an active terminator is that the current available on deassertion is independent of the voltage on the output of the terminator.

During deassertion the TL2218-285 operates as a 23.5 mA current source which is able to maintain this current level until the signal reaches the correct SCSI open circuit voltage. At this point the TL2218-285 becomes a voltage source of 2.85 V.



The additional current supplied by the TL2218-285 reduces the low-to-high transition time by ensuring that each voltage step is consistently the largest possible. The effect of this can be seen in figure 'First High Level Step Comparison', which shows the signal wave forms obtained after using a TL2218-285, a commercially available active terminator, and a passive termination network to terminate a 75 Ω cable (the equivalent of a heavily loaded bus). Even at 10 MHz the first step voltage of the TL2218-285 terminated system still exceeds the desired 2.0 V level.

Another feature of the TL2218-285 is the inclusion of a disable function which allows the terminator output to be shut down. This is particularly useful for a peripheral which finds itself somewhere other than the physical end of the bus, and needs some way of easily 'removing' it's terminator.

If disabled the TL2218-285 consumes just 500 µA of current, and maintains an output capacitance of 6 pF. Allowing for the 15 - 16 pF typical output capacitance of a peripherals transceivers, this will give a total node capacitance well within the 25 pF SCSI limit. An active terminator, on the other hand, will normally maintain a disabled output capacitance of 10 pF, often leaving the system to operate outside of the SCSI specification.

Use of the TL2218-285 also removes two possible causes of system failure or driver damage associated with active termination. Firstly the 2 % output tolerance of the TL2218-285 ensures it does not supply more current than allowed by the driver protecting SCSI limit. The tolerances of the voltage regulator and the 110 Ω resistors used in active termination, however, can result in the terminator supplying in excess of the 24 mA maximum.

The other potentially damaging situation arises when active negation drivers are being used. These devices sense bus voltages and source sufficient additional current to ensure that first step voltages reaches the minimum SCSI level. Despite this attractive feature their relatively high cost has limited their use to ultra fast changing control lines such as ACK and REQ.

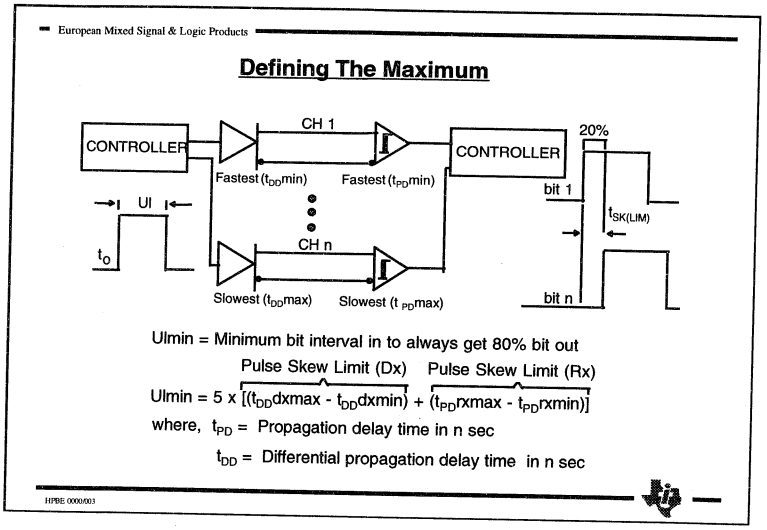
To be compatible with active negation drivers it is clear that any terminator connected to the bus must be able to sink current. Again this is a problem with active termination but not with either the TL2218-285 or a passive terminator. The voltage regulator of an active terminator will shutdown when any driver voltage exceeds 2.85 V. This allows the line voltage to rise and any driver which then pulls low may sink more than their 48 mA limit.

Current-Source Termination Using the SN75LBC968

There are numerous analog problems associated with driving the single-ended SCSI-bus and single-ended parallel busses in general. The SN75LBC968 addresses most of them. This device exhibits the analog performance to maximize first-step assertion levels in wired-OR lines and minimizes radiated emissions, crosstalk, and radiated emission susceptibility. The fundamental cause of the low first-step level is added loading of the bus with distributed capacitancefrom the attached devices. The '968 addresses this by offering a lower capacitance to the bus of only 13.5pF and nearly one-half of the maximum allowed by standard. The current mode termination of the '968 supplies a constant current to the line when the bus voltage falls below 2.5 V. This makes the termination current (and the next low-to-high voltage step) independent of the low level (asserted) bus voltage, unlike voltage-mode terminators. The constant current supplied by the '968 provides 16% more minimum current than Boulay termination and 33% more than passive termination. This extra current translates directly to first-step noise margin. The line drivers of the SN75LBC968 have a feature that was introduced into the SCSI standards to adress the first-step problem and is called active negation. The active negation is a controlled amount of output current from the driver during the transition from assertion to negation and is now required on the highest speed version of SCSI.

Since all single-ended SCSI drivers may not be as friendly as the '968, the receiver of this device has a noise filter and a large amount of input hysteresis to reject all but the wanted signals. The noise filter rejects voltage spikes less than 5ns while the 600mV of hysteresis rejects lower frequency noise with magnitudes below this level. These features not only help to reject crosstalk-induced noise, but make the bus less susceptible to noise from sources outside the bus as well.

Nine current-mode terminators have been integrated with nine-lines drivers and receivers that provides a common multiple to the byte-parity-arranged SCSI bus. With the nine control lines, an 8-bit SCSI bus can be implemented with two transceivers, a 16-bit bus with three, a 32-bit bus with five and so on. The other feature of this device, such as 3V-logic compatible inputs, power-up/-down glitch protection, and shrink small-outline packaging with flow-through architecture, make this an excellent solution to driving high-speed parallel data buses with single-ended signals.



High Speed Differential Parallel Communication

For multi channel systems consideration of the drivers differential transition time is not sufficient to determine the systems data rate capability. More specifically the difference in time between the slowest path and the fastest path within the system will set the limit.

There are many categories of delay in a differential system. This understanding is further complicated when you consider that a driver is really a single ended input to a differential output converter, while the receiver is a differential input to a single ended converter.

The propagation delay time is the time measured between the 50% level of the input pulse and the 50% level of the single ended output pulse. t_{PD}.

The differential propagation delay time is the time measured between the 50% level of the input pulse and 50% level of the differential output pulse t_{dD}.

The pulse skew of the driver is defined as the difference between the maximum differential propagation delay time and the minimum differential propagation delay them. The pulse skew of the receiver is defined as the difference between the maximum propagation delay time and the minimum propagation delay time.

As a rule of thumb the minimum unit interval can be defined as the bit interval time that ensures that always 80% of this bit interval appears at the output. The output bit interval in the worst case can be considered to have the skew limit deducted from the output bit interval. Therefore arithmetically the minimum unit interval can be defined as :

Minimum Unit Interval = 5 × (driver pulse skew + receiver pulse skew).

Hence the maximum operating speed of the communication system = 1 / Minimum Unit Interval

The Small Computer Systems Interface has overcome the problem of ensuring the speed of communication is guaranteed across parallel channels by defining skew limits within the specification. Lets review how this solution has been implemented.

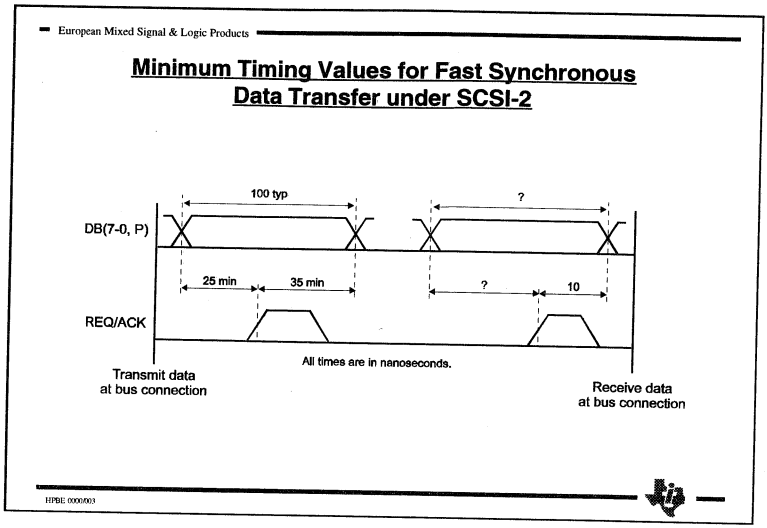
SCSI and Skew

SCSI is a parallel data bus. This means data is transferred over the cable more than one bit at a time. Both standards allow bus transfers as often as once every 100 ns or 10 million transfers per second.

Since the logical state of any one bit can change every 100 ns, this defines a period during which the logical state should be valid across the bus. This is the unit interval (UI). The voltage transitions that define the start and end of the UI can propagate along the bus at different velocities due to physical differences along each electrical path. This results in the UI to be different at the destination than at the origin.

Time variation of the defining voltage transitions is typically called skew. The limit for skew, designated $t_{sk(lim)}$, is the fastest minus the slowest propagation delays along any path of the bus. This will reduce the UI by $t_{sk(lim)}$ establishing a minimum unit interval (UI_{min}) that can be transmitted with a particular data bus.

The SN75976A1 and SN75LBC978 9-Channel Differential Transceivers are designed to operate at the fast-SCSI rates of 10 million transfers per second. Fast transfers are an option under SCSI-2 and SCSI-3. The following sections will attempt to show the skew budgeting required for a SCSI bus with these devices to assure standard compliance and interchangeability.



Minimum timing values for fast synchronous data transfer under SCSI-2

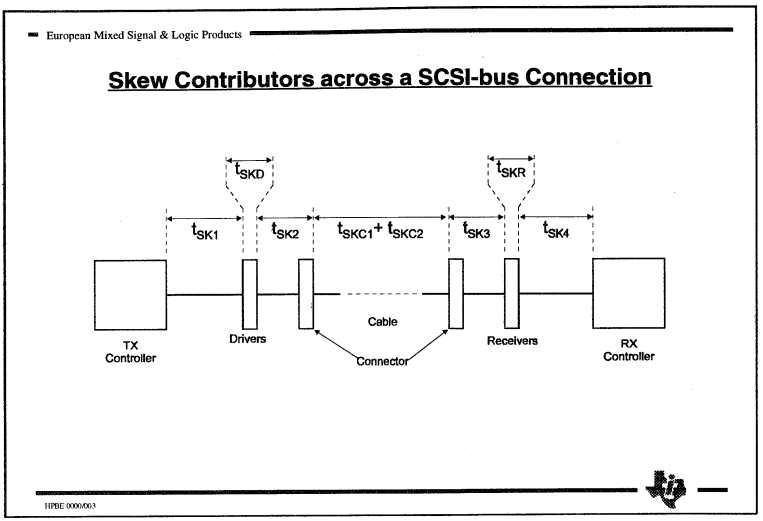
SCSI-2 (ANSI X3T9.2/86-109 rev 10h)

From *4.7 SCSI Bus Timing*, "*Unless otherwise indicated, the delay-time measurements for each SCSI device, shown in Table 7, shall be calculated from signal conditions existing at that SCSI devices own SCSI bus connection. Thus, these measurements (except cable skew delay) can be made without considering delays in the cable. ....*". Table 7 then defines the Fast Cable Skew Delay to be 5 ns, the Fast Deskew Delay to be 20 ns, and the Fast Hold Time to be 10 ns.

From *5.1.5.2 Synchronous Data Transfer*, "*... the target (initiator) shall first drive the DB(7-0,P) signals to their desired values, wait at least one deskew delay plus one cable skew delay, then assert the REQ (ACK) signals. The DB(7-0,P) signals shall be held valid for a minimum of one deskew delay plus one cable skew delay plus one hold time after the assertion of the REQ (ACK) signal. ... The target (initiator) shall read the value on the DB(7-0,P) signals within one hold time of the transition of the REQ (ACK) signal to true. ...*". This is interpreted literally and graphically in the picture above (Minimum timing values for fast synchronous data transfer under SCSI-2).

What do the timing requirements shown in figure 1 mean to a designer of a differential SCSI-2 compatible node?

First, time uncertainty or skew is caused by various factors that are shown in the next picture.



Skew contributors across a SCSI-bus connection

It is clear from the standard that transmitting fast synchronous data to a SCSI-2 bus requires a minimum of 25 ns set up time at the transmitting connector. This number will be defined by the transmitting controller's set up time (t_{TXSU}) less the skew of all the voltage transitions to the bus connector. Using the definitions of figure 2 and stating in equation form,

1. $t_{TXSU} - t_{SK1} - t_{SKD} - t_{SK2} \geq 25$ ns.

Since t_{SKD} is 8 ns for the SN75976A1, SCSI-2 requirements are met if

2. $t_{TXSU} - t_{SK1} - t_{SK2} \geq 17$ ns.

Similarly for the hold time requirement,

3. $t_{TXHD} - t_{SK1} - t_{SKD} - t_{SK2} \geq 35$ ns and

4. $t_{TXHD} - t_{SK1} - t_{SK2} \geq 28$ ns.

It is not as clear as to what timing is required at the receiving connector. One must dig further into the standard for clues about the set up and hold times with which you have to work. From Appendix B. Fast SCSI Skew Time, Figure 31 indicates that the sum of all skews from the transmitting connector to receiving SCSI controller are a Fast Cable Skew of 5 ns and a Fast Deskew Delay of 20 ns. Again stating this requirement in equation form,

5. $t_{SKC1} + t_{SKC2} + t_{SK3} + t_{SKR} + t_{SK4} \leq 5 + 20$ ns.

Substituting the SN75LBC976 receiver skew of 9 ns for t_{SKR}, a Fast Cable Skew for t_{SKC1}, and reducing equation 5 gives

6. $t_{SKC2} + t_{SK3} + t_{SK4} \leq 11$ ns.

(Note: The standard uses a 0 ns set up time for the receiving controller. A non-zero set up could be used but will subtract from the 11 ns.)

Although the standard wording implies that data must be read within 10 ns of REQ/ACK assertion at the receiving connector, it is also required that data be held for 35 ns at the transmitting connector. To derive the hold time available at the receiving controller (t_{RXHD}), the skews across the bus can be subtracted from the required transmit hold time.

7. $t_{RXHD} \geq 35 - t_{SKC1} - t_{SKC2} - t_{SK3} - t_{SKR} - t_{SK4}$

Substituting equation 5 into equation 7 gives

8. $t_{RXHD} \geq 35 - 25 \geq 10$ ns.

Therefore, compliance to the differential SCSI-2 standard with the SN75976A1 can be asserted with the following skew budget and controller receive hold time.

2. $t_{TXSU} - t_{SK1} - t_{SK2} \geq 17$ ns.

4. $t_{TXHD} - t_{SK1} - t_{SK2} \geq 28$ ns.

6. $t_{SKC2} + t_{SK3} + t_{SK4} \leq 11$ ns.

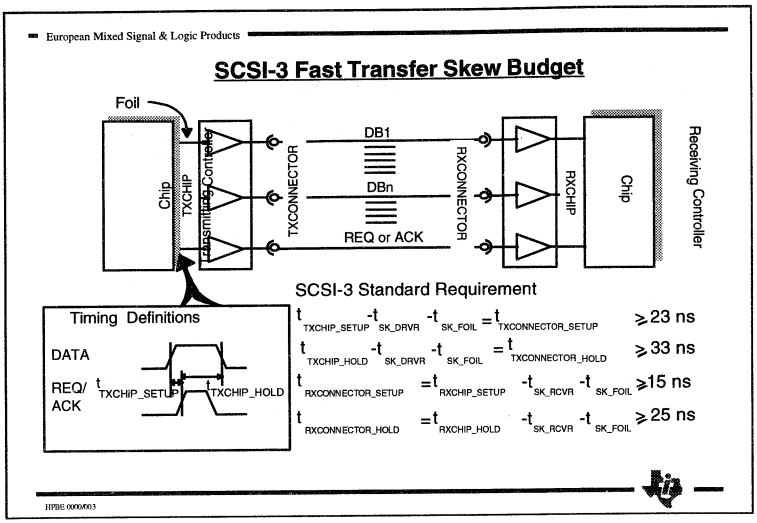
8. $t_{RXHD} \geq 10$ ns.

where, t_{TXSU} = SCSI controller's minimum transmit set up time at I/O pins
t_{TXHD} = SCSI controller's minimum transmit hold time at I/O pins
t_{RXHD} = SCSI controller's minimum receive hold time at I/O pins
t_{SK1} = transmit signal skew between the controller and 'LBC976
t_{SK2} = transmit signal skew between the 'LBC976 and SCSI-2 connector
t_{SK3} = receive signal skew between the controller and 'LBC976
t_{SK4} = receive signal skew between the 'LBC976 and SCSI-2 connector

As the designer attempts to meet these timing requirements, he or she will discover that the skew budget for t_{SK3} and t_{SK4} will depend upon t_{SKC2} which he or she ususally has no control over. For guidance here, we once again refer to appendix B of the standard. Figure 30 shows a bus skew budget example for a 25 m differential cable that allocates 5 ns for t_{SKC2}. This is not a "hard" requirement, but for the example bus, requirement 6 becomes,

6. $5 + t_{SK3} + t_{SK4} \leq 11$ ns or

6. $t_{SK3} + t_{SK4} \leq 6$ ns (remember, this is for a 0 ns receive data set up controller time. Subtract your controller's set up time from the 6 ns).



SCSI-3 Fast Transfer Skew Budget

SCSI-3 Parallel Interface (ANSI Working Draft X3T9.2 855D Rev 12a)

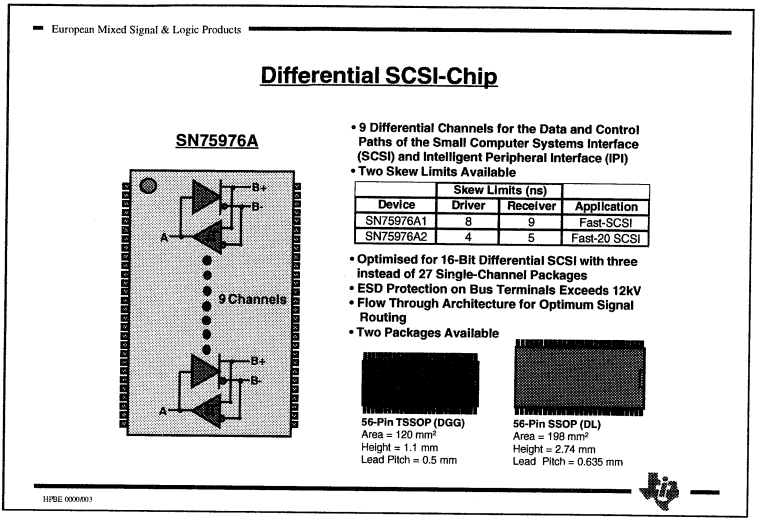
As you can imagine, assuring compliance to SCSI-2 can be open to interpretation of the standard's wording. The ambiguities of SCSI-2 for fast synchronous data transfer timing are being addressed in SCSI-3. This version of the standard requires specific set up and hold times at the SCSI-3 connector. These are

Transmit set up time	≤	23 ns
Transmit hold time	≥	33 ns
Receive set up time	≤	15 ns
Receive hold time	≥	25 ns.

The budget behind the connector is left to the implementor and depends upon the controller, transceivers, and layout being used. Table 1 shows some skew budget examples with various controller chips that would comply with the requirements at the SCSI-3 connector. The column under "Rec" (for recommended) is data for the worst case numbers for SCSI controllers surveyed by the SCSI SPI Working Group and budgets 8 ns for the external driver and 9 ns for the external receiver. This is origin of the $t_{sk(lim)}$ specifications in the SN75LBC976 data sheet.

Parameter	Rec	Vendor A	Vendor B	Vendor C	Units
min Tx_controller_setup =	32	30	35	35	ns
min Tx_controller_hold =	42	42	45	45	ns
min Rx_controller_setup =	5	0	5	0	ns
min Rx_controller_hold =	15	20	15	10	ns
tsk_etch =	1	1	1	1	ns
max tsk_dvr =	8	6	11	11	ns
max tsk_rvc =	9	4	9	14	ns

Table 1. Transceiver skew budgets for various SCSI controllers.



SN75976A1/A2 Two Chip Differential SCSI

Much debate has taken place on differential versus single ended SCSI for data rates above 5 million transfers per second (MTps). It is clear however, that for data rates approaching 10 MTps and at line lengths in excess of 6 metres, differential SCSI is essential.

As we discussed earlier, the standard 8-bit interface is made up of 8 data lines, one parity bit, and 9 control lines, making 18 channels in total. The only differential transceivers capable of transmitting at 10 MTps data rate have utilised the LS and ALS technologies. Using these technologies and considering the 18 transceivers per interface the power consumption is quite considerable, 2.4 W with all drivers disabled. Turn the drivers on and the power consumption rises to nearly 4 W.

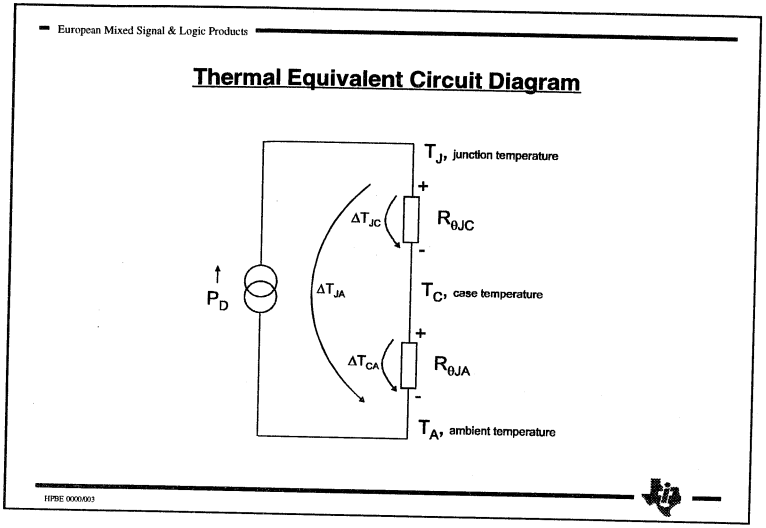
From a designers viewpoint, 2.4 watts is a considerable amount of heat to remove from a system. This is evident in the case of compact hard disk drives where shear equipment size is the limiting element. A further factor is board area, using one discrete transceiver per channel, i.e. 18 8-pin SO packages, is unacceptable for many applications.

From a semiconductor designers viewpoint integrating a number of transceivers is of course possible however the limiting factor once again is power dissipation. The SN75976A1/A2 is designed to overcome both the problems of power dissipation and integration. The device incorporates on a single IC, nine RS-485 configurable transceivers each capable of transmitting at 10 MTps ('976A1) or 20 MTps ('976A2). This is made possible using LinBiCMOS* technology. With all drivers disabled the quiescent current of the '976A1/A2 is typical 8mA., a considerable saving over LS and ALS parts. The package size has also been reduced to a minimum using the 56 pin SSOP package (0.635 mm pitch) or the Shrinked Widebus (0.5 mm pitch), which reduces board area significantly compared with alternate packages such as PLCC. The reader should note that irrespective of the device power, there is still the relatively high line current.

The SN75976A1/A2 is fully configurable to facilitate connection to any type of SCSI system arrangement. The 9 channels can be arranged into seven possible channel functions using the BSR, CDE0, CDE1, CDE2, CRE control pins.

The 7 channel configurations are:

1. Transparent, permanently enabled Receiver.
2. Transparent, permanently enabled Driver.
3. Bi-directional transceiver with direction control.
4. Driver with enable control.
5. Open ended driver for Wired OR control lines.
6. Driver with ORed data and enable lines.
7. Permanent high impedance state.



Thermal Equivalent Circuit Diagram

Since the SN75976A is a chip which integrates nine differential channels, it is important to analyse the power consumption and the resulting junction temperature, which has a limit of 150°C. The picture above shows the thermal equivalent circuit diagram, which is useful to calculate the junction temperature for a specific operating condition. $R_{\theta JC}$ is the junction-to-case thermal resistance and $R_{\theta CA}$ is the junction-to-case thermal resistance. $R_{\theta JA}$, equals the junction-to-ambient resistance and equals $R_{\theta JC} + R_{\theta CA}$.

The mean junction temperature can be calculated using the relationship:

$$T_J = R_{\theta JA} \times P_D + T_A$$

The junction temperature rise ΔT_J above ambient temperature is:

$$\Delta T_J = T_J - T_A = R_{\theta JA} \times P_D$$

The following pages cover a complete thermal analysis for the SN75976A 9-channel differential transceiver.

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Power and Temperature Consideration of the SN75976A

Parameter	Typical	Maximum	Units
P_{D1}, Power dissipation when transmitting at 20 MXfers/s	1104.8	1700.2	mW
P_{D2}, Power dissipation when receiving data at 20 MXfers/s	210.6	428.5	mW
P_{D3}, Power dissipation with all drivers asserted	1251.5	1821.0	mW

Parameter		Typical	Maximum	Units
ΔT_{J1},	Junction temperature rise when transmitting at 20 MXfers/s	55.2	85.0	°C
ΔT_{J2},	Junction temperature rise when receiving data at 20 MXfers/s	10.5	21.4	°C
ΔT_{J3},	Junction temperature rise with all drivers asserted continuously	62.6	90.9	°C

Transmit	Receive	Mean T_J, °C		
		T_A = 25°C	T_A = 55°C	T_A = 70°C
100%	0%	80.2	110.2	125.2
67%	33%	65.4	95.4	110.4
50%	50%	57.9	87.9	102.9
33%	67%	50.3	80.3	95.3
0%	100%	35.5	65.5	80.5

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SN75976A 9-Channel Differential Transceiver Thermal Analysis

The following pages analyze the power consumption and the junction temperatures of the SN75976A1DL, SN75976A2DL, SN75976A1DGG, or SN75976A2DGG 9-Channel Differential Transceivers in typical applications.

Power dissipation

Power is dissipated within the silicon from three primary sources; the steady-state quiescent power, ac or switching power, and dc or resistive losses in the output drivers.

Steady-State Quiescent Power

The current necessary to bias the circuits of '976A with all nine channels enabled as differential drivers is typically 39.7 mA with a maximum test limit of 60 mA. When the device is enabled to be nine differential receivers, I_{CC} becomes 25.2 mA typically with a maximum limit of 45 mA. These values are from statistical characterization of seven different wafer lots over a supply voltage range of 4.75 V to 5.25 V and a case temperature range of 0°C to 125°C.

Driver quiescent power:

P_{DCC} = $I_{CC} \times V_{CC}$

= 39.7 mA x 5.0 V = 198.5 mW average

< 60.0 mA x 5.3 V = 318.0 mW maximum

Receiver quiescent power:

P_{RCC} = $I_{CC} \times V_{CC}$

= 25.2 mA x 5.0 V = 126.0 mW average

< 45.0 mA x 5.3 V = 238.5 mW maximum

Switching Power

The average increase in the average I_{CC} for an unloaded driver of the SN75976A was measured on four representative samples. The average increase was 4.88 mA/Channel when switching at 10 MHz (20 MXfers/s), a 50% duty cycle, and at a V_{CC} of 5 V. At a V_{CC} of 5.25 the single largest measured increase was 5.3 mA/Channel.

One driver's switching loss at 10 MHz:

$$P_{DAC} = I_{CC} \times V_{CC}$$
$$= 4.9 \times 5.0$$
$$= 24.4 \text{ mW/Channel typical}$$
$$\text{and} \quad < 27.8 \text{ mW/Channel maximum.}$$

A receiver, switching at the same frequency and duty cycle with unloaded outputs, consumed an additional 2.0 mA/Channel above steady-state on average. The maximum was 2.5 mA/Channel on one sample at a V_{CC} of 5.25 V.

One receiver's switching loss at 10 MHz:

$$P_{RAC} = I_{CC} \times V_{CC}$$
$$= 2.0 \times 5.0$$
$$= 10.0 \text{ mW/Channel typical}$$
$$\text{and} \quad < 13.1 \text{ mW/Channel maximum.}$$

DC Losses

The output stage losses vary with either the magnitude of the output voltages, the output transistor saturation or drain-to-source voltages, and with the load conditions. The following is derived from the solution of the equivalent circuit of a differential SCSI bus and no further proof is included in this analysis.

The typical single-ended output voltages of the '976A driver have been characterized with a SCSI load test circuit with the following results.

Parameter	Typical[1]	Worst Case[2]
VO+, "+" SCSI line voltage when asserted	1.5 V	1.3 V
VO+, "+" SCSI line voltage when negated	3	3.7
VO-, "-" SCSI line voltage when asserted	1.6	1.5
VO-, "-" SCSI line voltage when negated	3.3	3.9
VOD, differential output voltage when asserted	1.4	-2.2
VOD, differential output voltage when negated	-1.8	-2.6

Table 1: SN75976A output voltages with a SCSI load.

Solution of the circuit with the SCSI test load and the voltages in Table 1 results in a typical power dissipation in the output transistors of 117 mW when asserted and 60 mW when negated. The worst case power is 167 mW asserted and 113 mW negated.

Driver output dc losses:

$$P_{DOH} < 167.0 \text{ mW/Channel maximum}$$
$$P_{DOH} = 117.0 \text{ mW/Channel typical}$$
$$P_{DOL} < 113.0 \text{ mW/Channel maximum}$$
$$P_{DOL} = 60.0 \text{ mW/Channel typical}$$

At an I_{OL} of 8 mA, the typical receiver V_{OL} is 0.6 V with a maximum test limit of 0.8 V. At -8 mA, the typical V_{OH} is 4.5 V with a minimum limit of 2.4 V.

[1]*Typical* is the statistical average of the measurements on 268 samples from seven wafer lots at a case temperature of 25°C and a V_{CC} of 5 V.

[2]*Worst Case* is the maximum differential output voltage measured on 268 samples from seven wafer lots at a case temperature of 125°C and a V_{CC} of 5.25 V.

Receiver output dc losses:

P_{ROH} = I_{OH} x (V_{CC} - V_{OH})
= 8 mA x (5 V - 4.5 V)
= 4.0 mW/Channel typical
< 8 mA x (5.3 V - 2.4 V)
< 23.2 mW/Channel maximum

P_{ROL} = I_{OL} x V_{OL}
= 8 mA x V
= 4.8 mW/Channel typical
< 8 mA x 0.8 V
< 6.4 mW/Channel maximum

The components of the power dissipation in the SN75976A are summarized in Table 2.

Parameter	Typical	Maximum	Units
P_{DCC}, Steady-state quiescent power for 9 drivers	198.5	315.0	mW
P_{DAC}, Switching power for 1 driver at 10 MHz	24.4	27.8	mW/Channel
P_{DOH}, Driver output power loss when asserted	117.0	167.0	mW/Channel
P_{DOL}, Driver output power loss when negated	60.0	113.0	mW/Channel
P_{RCC}, Steady-state quiescent power for 9 receivers	126.0	238.5	mW
P_{RAC}, Switching power for 1 receiver at 10 MHz	10.0	13.1	mW/Channel
P_{ROH}, Receiver output power loss when asserted	4.0	23.2	mW/Channel
P_{ROL}, Receiver output power loss when negated	4.8	6.4	mW/Channel

Table 2: Components of power dissipation.

DEVICE POWER DISSIPATION

To determine the total power that will be dissipated in the package, the operation of the device and the power component contributions must be evaluated. The steady-state quiescent power is a constant, but the switching power and output stage power will depend upon the data being transmitted or received and the duration of the transfer. Three cases will be analyzed; 1) nine channels continuously transmitting random data to a Fast-20 SCSI bus, 2) nine channels continuously receiving random data from a Fast-20 SCSI bus, and 3) the unlikely assertion of all nine bits continuously.

Since the assumption in case 1) and 2) is random data, the probability that any one bit on the bus is asserted is equal to the probability of it being negated. With equal probability and a long observation period relative to the data transfer period, the mean power in an output stage will be the average of the high-level and low-level values. For nine channels and the three cases;

case 1) $P_{DO1} = (P_{DOH} + P_{DOL})/2 \times 9$,

case 2) $P_{RO2} = (P_{ROH} + P_{ROL})/2 \times 9$, and

case 3) the driver outputs are continuously asserting the bus so, $P_{DO3} = P_{DOH} \times 9$.

The circuit switching losses, P_{DAC} and P_{RAC}, were measured with the switching loss occurring on every cycle. Because the state of the output is random and nondeterministic, the probability that the driver output will change state on the next cycle is equal to the probability that it will not. Again, over a long observation period the mean switching power for each operating case is

cases 1) $P_{DAC1} = P_{DAC}/2 \times 9$

case 2) $P_{RAC2} = P_{RAC}/2.x\ 9$

case 3), where there is no switching power component, $P_{DAC3} = 0$.

The power dissipated in the package for the three cases is then

$P_{DI} = P_{DCC} + (P_{DOH} + P_{DOL})/2 \times 9 + P_{DAC}/2 \times 9$

Continuously is defined here as at least three device thermal time constants or approximately 15 seconds.

$P_{D2} = P_{RCC} + (P_{ROH} + P_{ROL})/2 \times 9 + P_{RAC}/2 \times 9$

$P_{D3} = P_{DCC} + P_{DOH} \times 9$.

Parameter	Typical	Maximum	Units
P_{D1}, Power dissipation when transmitting at 20 MXfers/s	1104.8	1700.2	mW
P_{D2}, Power dissipation when receiving data at 20 MXfers/s	210.6	428.5	mW
P_{D3}, Power dissipation with all drivers asserted	1251.5	1821.0	mW

Table 3: Device power for three cases.

JUNCTION TEMPERATURE

Measurements of the SSOP-56 package and leadframe used on the SN75976ADL were performed on a 13.0 cm by 9.8 cm six-layer printed circuit board. The board was built with the ground and heat-sinking pins soldered to individual pads and connected to a second layer ground plane through 0.15 mm etch runs. There was one common via interconnect per side. The ground plane was 0.254 mm below the surface of the 1.6 mm thick board and was a 1 oz. copper layer. The results of tests on two samples were an average $R_{\theta JA}$ of 49.7°C/W with one Watt of power dissipation and no air flow.

Measurements on six TSSOP-56 packages and leadframes used on the SN75976ADGG were performed. The test board was 13.7 cm by 8 cm by 1 mm thick with a ground and V_{CC} plane of 1 oz. copper. The ground and heat-sinking pins were soldered to individual pads and connected to the ground plane through 0.15 mm etch runs and one common via interconnect per side. The results of the test was an average $R_{\theta JA}$'s of 46.7°C/W with one Watt of power dissipation and no air flow.

Using a rounded 50°C/W for each package, the mean junction temperature rise above ambient can then be calculated. Table 4 shows the results for each case using the relationship:

$$\Delta T_J = T_J - T_A = R_{\theta JA} \times P_D$$

Parameter		Typical	Maximum	Units
ΔT_{J1},	Junction temperature rise when transmitting at 20 MXfers/s	55.2	85.0	°C
ΔT_{J2},	Junction temperature rise when receiving data at 20 MXfers/s	10.5	21.4	°C
ΔT_{J3},	Junction temperature rise with all drivers asserted continuously	62.6	90.9	°C

Table 4: Estimated junction temperature rise above the ambient still-air temperature.

CONCLUSION

Most designs require two junction temperature restrictions.
1) The junction operating temperature should not exceed 150°C under worst case operating conditions and
2) the mean operating junction temperature should be no more than 110°C.

The junction temperature rise above the ambient still-air temperature is estimated in Table 4 for three operating conditions. The worst-case temperature rise is T_{J3} and is applicable to requirement 1). Written in equation form and solving for T_A,

$T_A + T_{J3} < 150°C$
$T_A < 150°C - T_{J3}$
$T_A < 150°C - 90.9°C = 59.1°C.$

Evaluation of the mean operating junction temperature can vary a great deal based upon the assumptions of mean still-air temperature and transmit-to-receive duty cycles. In any case, the use of the typical values T_{J1} and T_{J2} are required. The following table calculates the projected mean junction temperature for various duty cycles and ambient air temperatures.

		Mean T_J, °C		
Transmit	Receive	T_A = 25°C	T_A = 55°C	T_A = 70°C
100%	0%	80.2	110.2	125.2
67%	33%	65.4	95.4	110.4
50%	50%	57.9	87.9	102.9
33%	67%	50.3	80.3	95.3
0%	100%	35.5	65.5	80.5

Table 5: Projected mean junction temperatures vs. duty cycles and ambient air temperature.

With the parameters defined above, the SN75976A, in either offered package, will meet the design requirements up to a maximum ambient still-air temperature of 60°C under a worst-case scenario of all nine drivers enabled and continuously asserting all lines of a Differential SCSI bus with 32 nodes.

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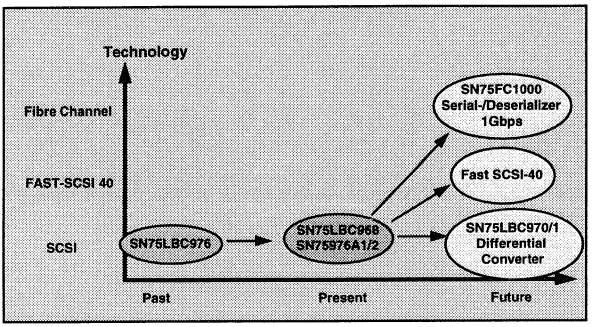
Computer Differential Product Roadmap



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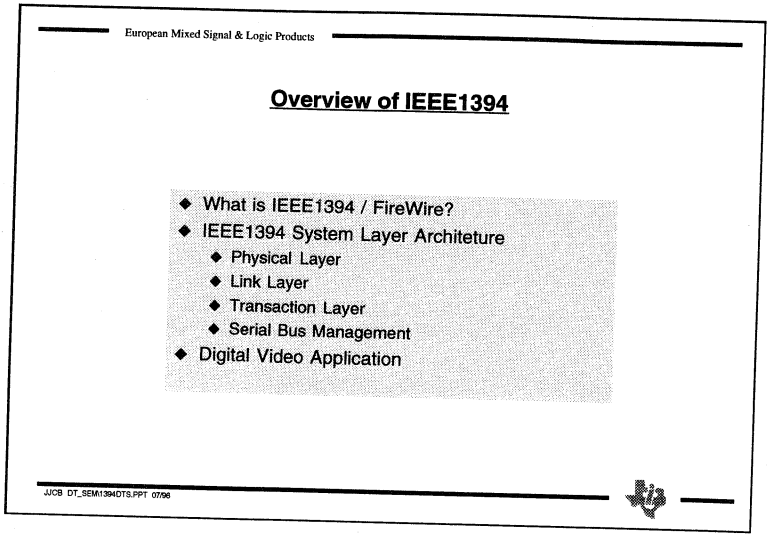
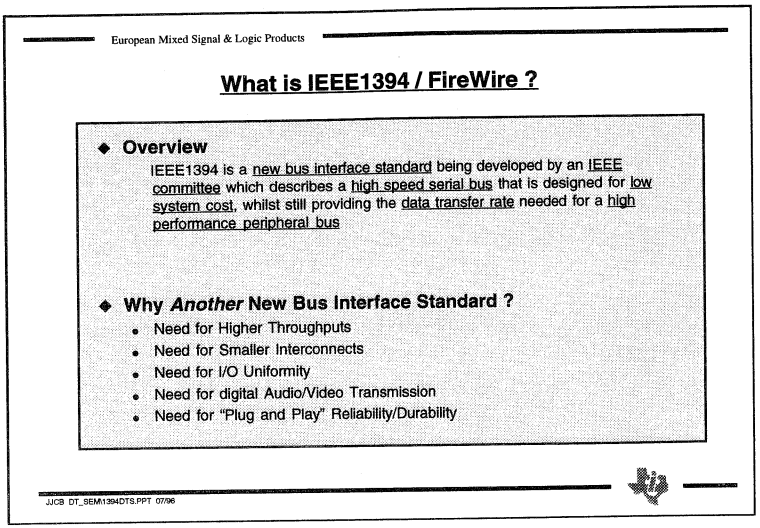


Another advanced high speed interfaces is the IEEE 1394 (Firewire). For applications requiring very high data rates, like digital video, the IEEE 1394 standard has been defined. This standard describes a low-cost, high-performance serial bus supporting data rates of 100, 200 and 400 Mbits/s. This paragraph of the data transmission seminar covers after an 1394 overview, the system layer architecture and protocol of this interface and a representative design example, a digital video application.

The IEEE 1394 High Performance Serial Bus is designed for any application in a data communication environment, including:

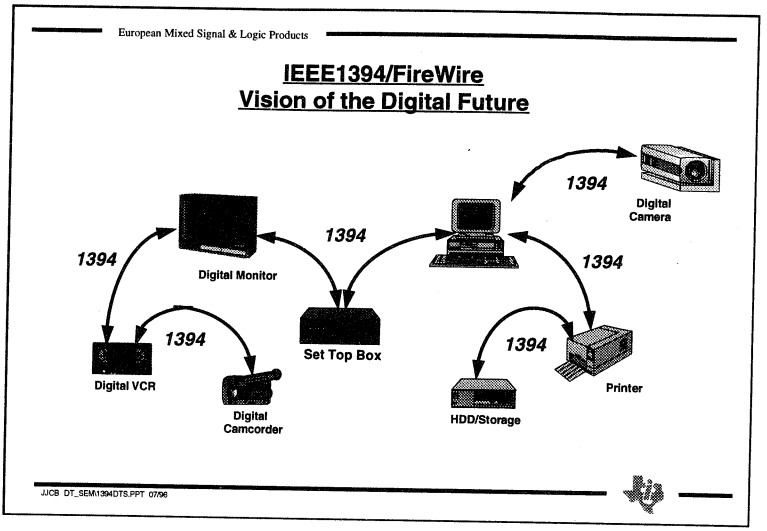
- Computers, both desktop and portable
- Consumer electronics products such as: Set-top boxes, VCRs, camcorders, digital video disk (DVD) and digital TVs
- Multimedia products such as digital cameras, video editing machines, and stereo/audio equipment
- Electronic publishing products such as printers and scanners
- Data storage and retrieval products such as hard disk drives and CD-ROMs
- Industrial equipment, using high speed, time critical data transmission



IEEE 1394 is an emerging IEEE bus interface standard for portable and desktop computing environment. It provides an important linking technology which bridges the consumer and computer markets, and facilities the new digital 'information-highway'. The standard describes a serial bus driven by an advanced communication protocol which is designed for low system cost while providing the data transfer rate needed for a high-performance peripheral bus. Because of the inherent advantages that IEEE 1394 possesses, it is well positioned to become the interface standard of the future.

Why a New Bus Interface Standard?

Existing bus interface solutions do not address many of the needs that systems of the future will require. For example, emerging applications such as multimedia interfacing will require much faster data transmission rates, lower cable costs and the ability to transmit data in 'real-time'. Other potential needs include a need for reliability and durability, smaller interconnects, and a universal interconnect solution. The IEEE 1394 technology is designed to address these emerging needs as well as many others.



Why is this 'vision' desirable ?

More and more the use of computer based equipment in private households requires an interface solution for the home and home office networking.

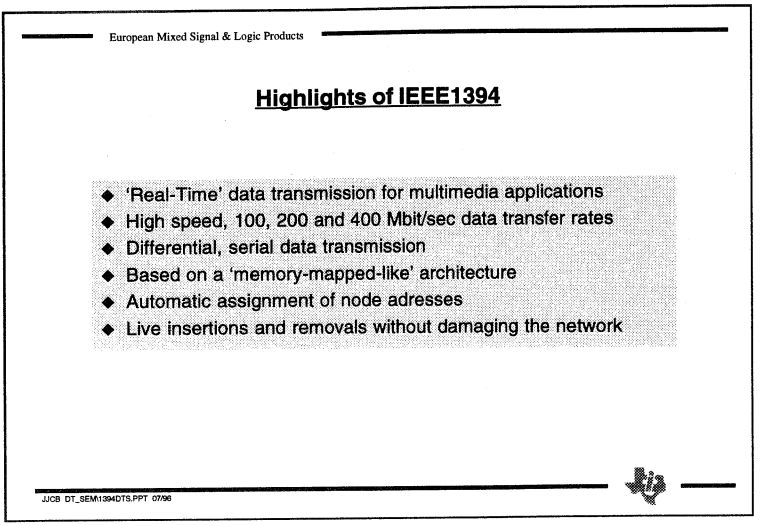
This is enforced by the evolving market of digital TV broadcasts, interactive services, games, and home shopping. The introduction of digital set top boxes, which enable the reception of these services beside digital TV, expects the capability of the digital interface to the PC, storage media and later to the TV.

Another consumer equipement, the digital camcorders and digital VCR transmitting digital video enables now home video editing without any losses.

The increasing acceptance of the videoconferencing technology shows again another application where the use of digital video transmission increases the video quality, whilst decreasing the system costs

Why is 1394 relevant to this market ?

It is the *only* interconnect solution designed to be used accross multiple end equipments and provides a *single interface* for audio, video and control. Due to the specification by international committees, 1394 is a *non-proprietry* international standard. The '*hot insertion*' capabilities enhance ease of use, which is today the highest requirement for end-user of multimedia equipment.



'Real-Time' Data Transfers

Key enabling feature of IEEE 1394 is the ability to support a low overhead, guaranteed bandwidth. This capability is extremely important for applications in which time-sensitive transfers are needed, such as digital audio and video applications. This feature is one of the reasons why IEEE 1394 is well-suited as a multimedia interface for both the computer and consumer environments.

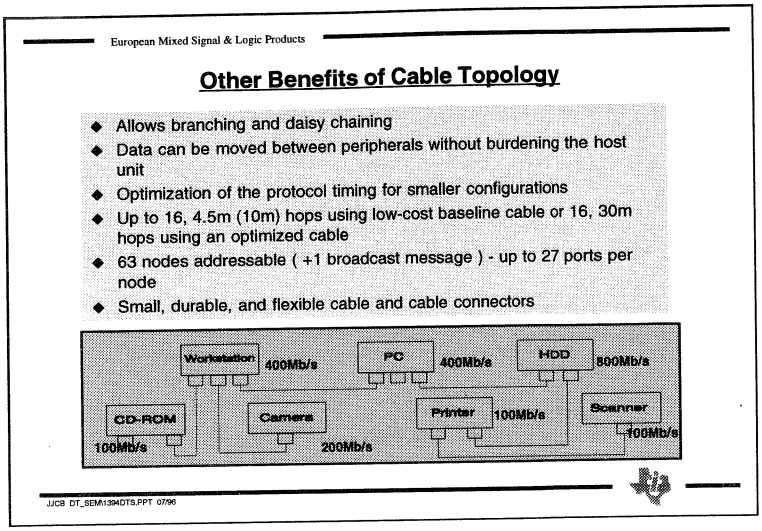
High Speed Serial Bus

Data rates of 100, 200 and 400Mbit/sec across the cable medium are supported in the current standard. Additionally all future speed improvements will be made backwardly compatible with previous speeds. This will allow a scaleable topology capable of supporting multiple speeds. For example the IEEE 1394-1995 architecture will support 100, 200 and 400 Mbit/sec nodes in the same network. As technology changes and data rates of 1394 increases, it will remain compatible with previous speeds, because the 1394 protocol is speed independent.

Ease of Use

IEEE 1394 is also a true 'hot-insertion' hardware solution. 'Live' cable insertions and removals can be performed without damaging the network (hot-plugging).

The IEEE 1394 protocol automatically reconfigures the network whenever a node is added or removed from the network. Since IEEE 1394 is a point-to-point bus technology, active termination is not needed. IEEE 1394 is based on a 'memory-mapped-like' architecture in which all resources are viewed as a memory location. This makes data transactions more efficient, and simplifies software driver designs. There is no need for address switches due to the automatic assignment of node addresses.



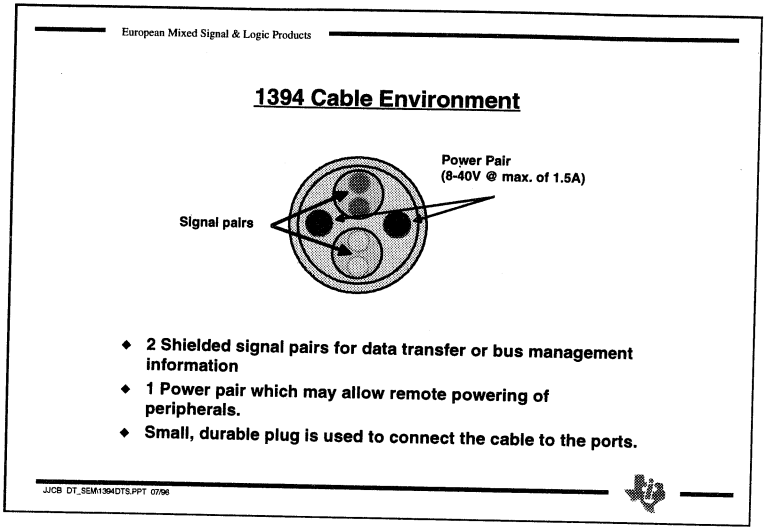
Flexible Topology

The IEEE 1394 cable topology enables both branching and daisy-chaining of nodes. Automatic optimization of protocol timing for smaller configurations is also supported for improved performance. Additionally, data can be moved between peripherals without burdening the host unit. That means that the host of a node sitting between two communication partner won't be involved in the data delivery.

The combination of these advantages make IEEE 1394 a true peer-to-peer communication standard.

With repeater 72 m of cabling distance between two devices is possible. A repeater function can be implemented by simply using the physical layer powered through the 1394 cable. Studies are currently improving the cable length, whereas a 10m cable is already possible.

The maximum address space of one bus is limited by 64 and furthermore 1024 different busses, each with 63 nodes (+1 broadcast message), can be addressed using the branching topology.

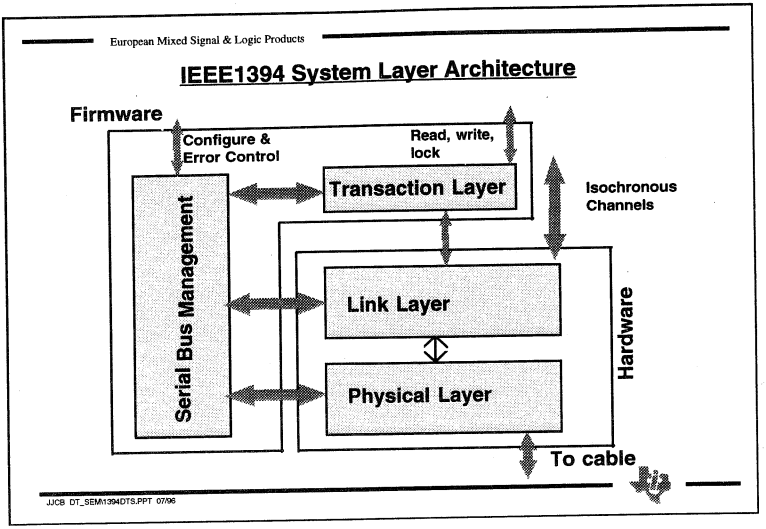


Cable and Connectors

Since data is transmitted serially in IEEE 1394, the need for wide, expensive multiconductor cables and connectors is eliminated. In its place are small, flexible and inexpensive cables and cable connectors. The cable used is a 6-wire, shielded twisted-pair with 4 lines dedicated for data and control information and two lines for carrying power. This power pair ensures that the integrity of the network maintained if a power-down situation occurs within a node. In addition low power devices like a digital videoconferencing camera may be powered through the 1394 medium, eliminating the need for a separate power source.

A rugged, durable connector allows multiple cable insertions and removals (up to 5000).

The specification of cable and connectors is included in the IEEE1394-1995 standard.

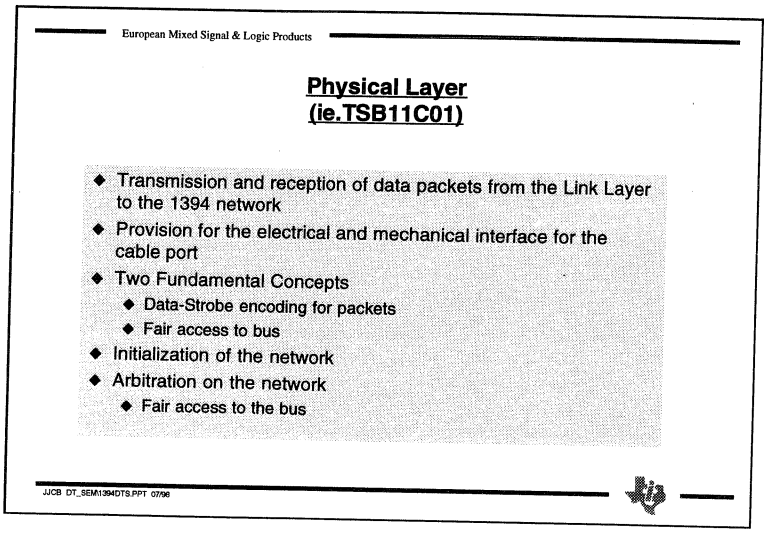


The phy and the link are the hardware applications of 1394 and provide the direct interface to the cable environment as well as isochronous channels. Texas Instruments has developes the chipsets to control the cabling which is made up of the

Physical Layer : ie. TSB11C01, TSB14C01, TSB21LV03

Link Layer : ie. TSB12C01A, TSB12LV21, TSB12LV31

The software control of this hardware is implemented by the system layer architecture: serial bus management, and transaction layer.



The physical layer is the interface between the 1394 cable network and the 1394 Link Layer and is providing the transmission and reception of data, which are addressed for this dedicated node.

On the 1394 cable network side, the analog transceiver function is necessary to implement ie. for the TSB11C01 a 3 port node supporting 100Mb/s for a multi-port interface between different 1394 end equipments. Each cable port incorporates two differential line transceiver.

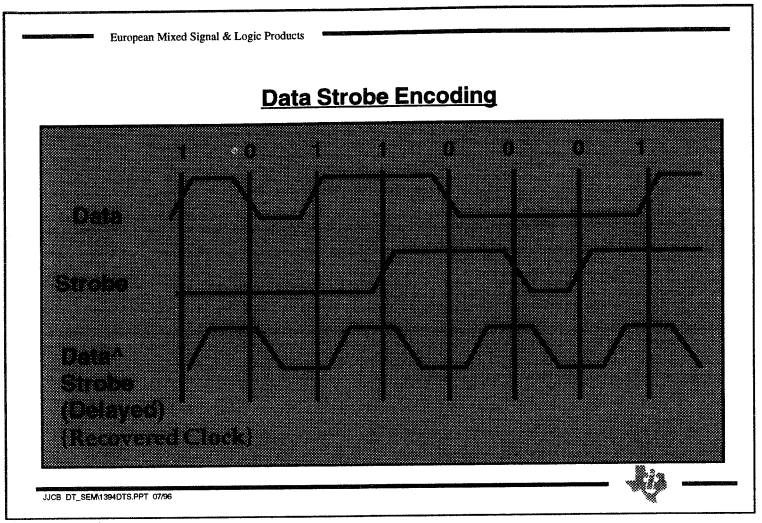
The differential output voltage is limited between 180 mV and 260 mV, by a common-mode voltage range between 1.12 V and 2.54 V.

During transmission, one node has access to the bus. Operation may occur in half duplex mode using two signals:

★Data

★Strobe

The transceivers include circuitry to monitor the line conditions, needing for determining connection status, for initialization and arbitration, and for packet reception and transmission.



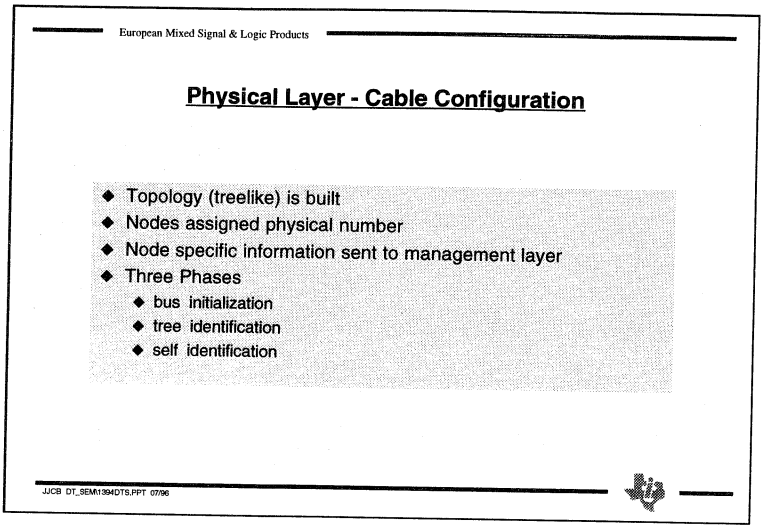
The data^strobe signal created from the exclusive or is a reconstructive clock.

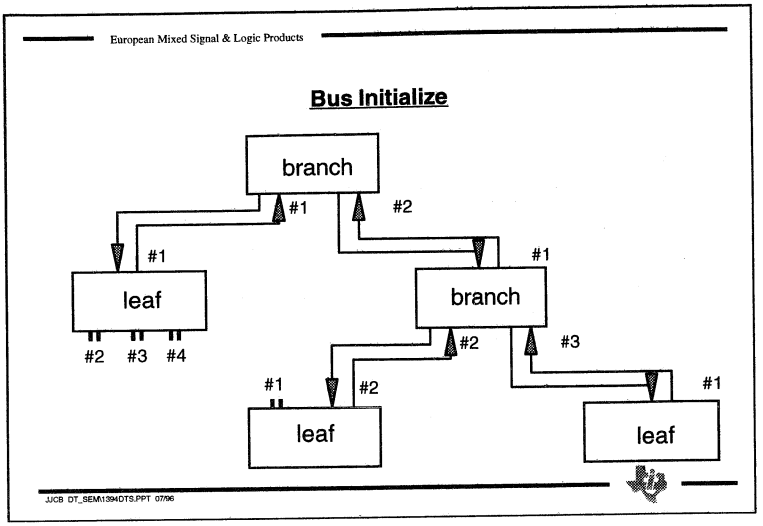
Data transmits NRZ (Non return to zero)

Strobe changes state for two alike consecutive NRZ data bits

Ensures transition occurs on either of the data or strobe lines one bit period apart for higher skew tolerance

Data^Strobe created by exclusive-or for internal clock


European Mixed Signal & Logic Products
Physical Layer - Cable Configuration
Topology (treelike) is built
Nodes assigned physical number
Node specific information sent to management layer
Three Phases
bus initialization
tree identification
self identification
JJCB DT_SEM1394DTS.PPT 07/96

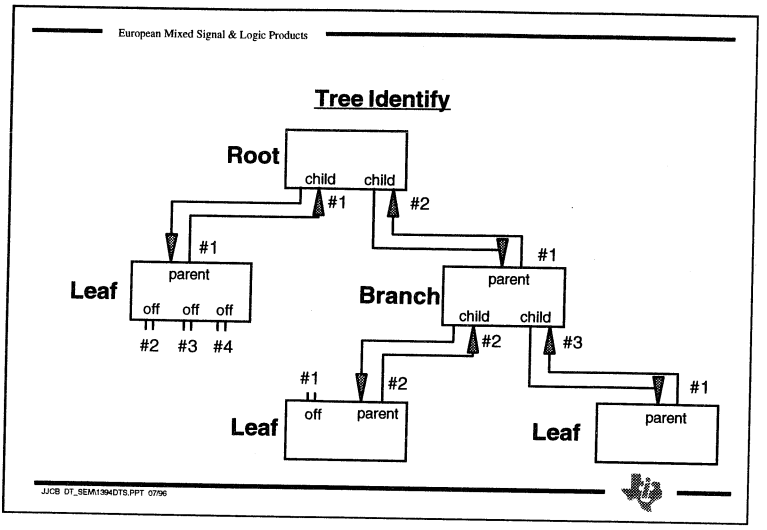


Node joining the bus:

A bus reset signal forces all nodes into a state that clears all the topology information and starts the next phase.

After initialization, each node only has information stating whether it is a:

1. Branch - more than one directly connected neighbor
2. Leaf - only a single neighbor OR
3. Isolated - unconnected

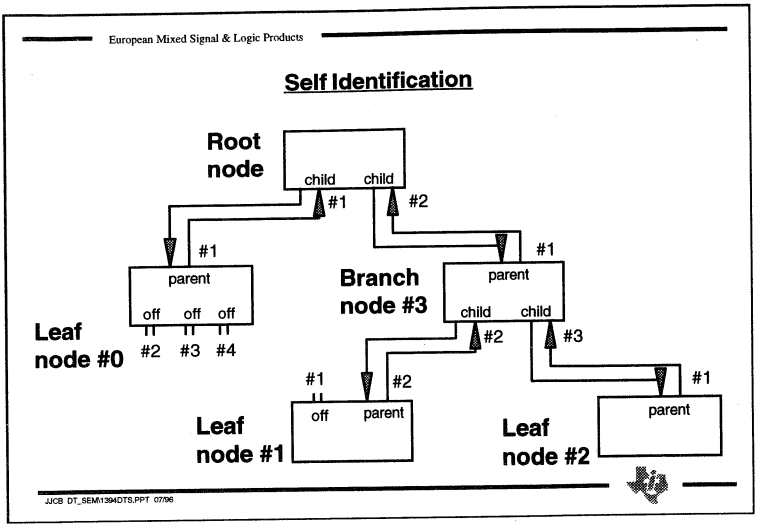


Tree ID:

Translates the general network topology into a "tree". One node is designated the ROOT and all other physical connections have a direction associated with them pointing towards the root node as a :

1. Parent - connected port of a node closer to the root node
2. Child - connected port further from the root OR
3. Off - unconnected port which does not participate in any further arbitration

The benefit is to optimize timing performance and to set up the topology from the root node to realize arbitration methods.



Self Identity:

What?

Each node selects a unique physical ID and identifies itself to attached management entities (firmware). This allows low level power management and the building of a system topology map.

How?

Transmitting 1 to 4 short packets at the base rate onto the cable that has the physical ID and some management information.

The ID is the count of the # of times a node passes through the state of receiving self-ID information before actually receiving it's own.

NOTE: a node is not required to decode packets, just to count ID sequences since bus initialization

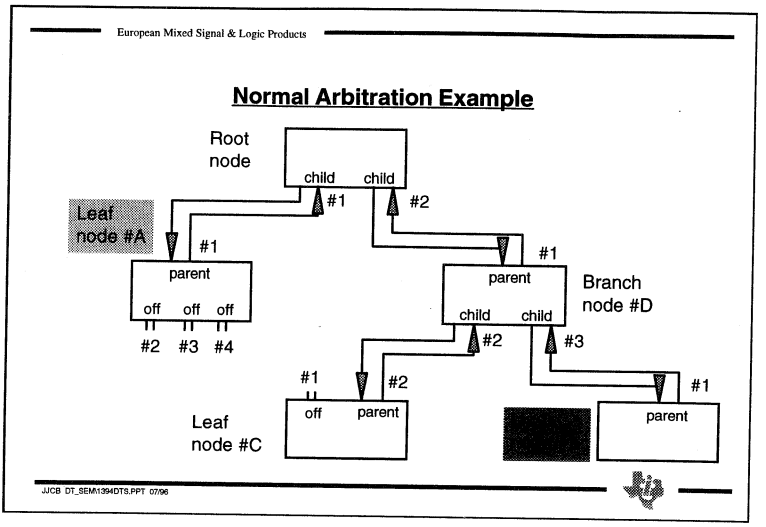
Process:

1. Root node passes control of the media to the node attached to its lowest numbered connected port.

2. Root waits for "ident-done" signal - parent and children of node have then all identified themselves.

3. Control passes to next highest port etc.

NOTE: Ch-i means the node attached to that port is now identified



EXAMPLE:

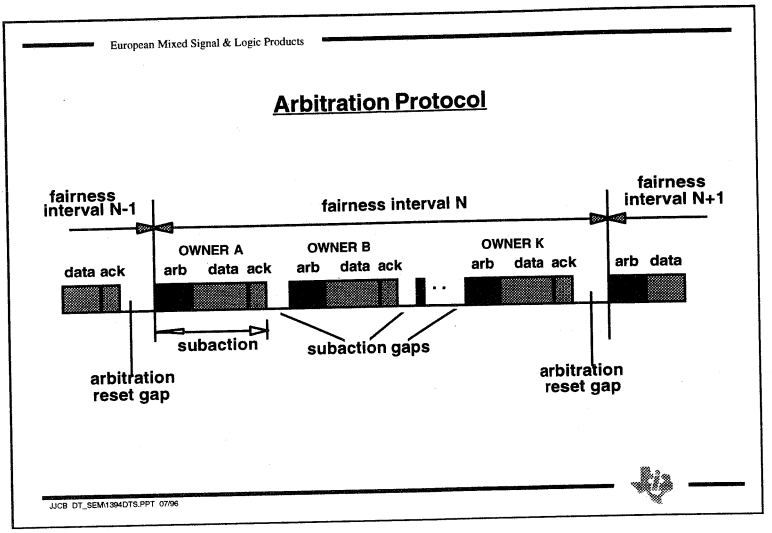
1. Nodes A and E begin arbitrating at the same time by sending a request to their parents

2. Parent node (D) of node E forwards the request to its parent (B) and denies access to it's other children (C) by sending a data_prefix, while parent of node A is denying access to it's other children.

3. The root grants access to the first request (node A), while the other parent (D) acknowledges the deny by withdrawing its request and passing on the deny.

4. Node E then withdraws its request. Node A receives the grant and sends a data_prefix signal to warn all nodes that data is to be sent.

Note: Node E will gain access to the bus according to the fairness interval.

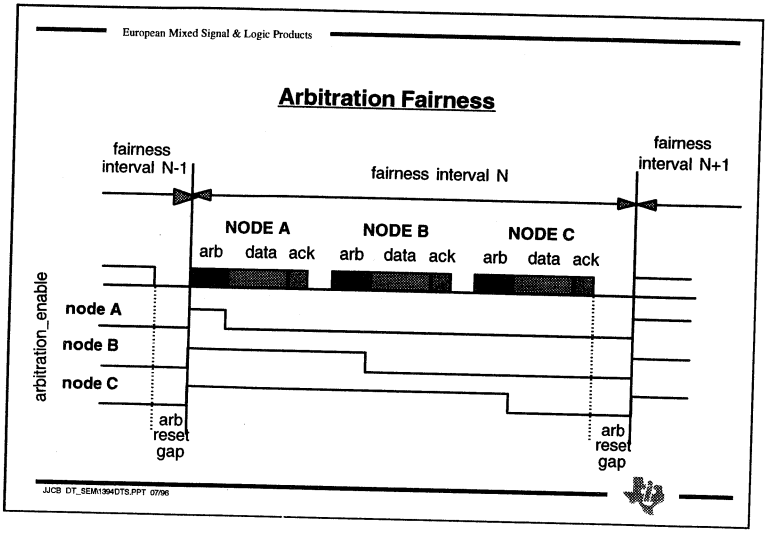


Normal cable arbitration methods guarantee that only one node will be transmitting at the end of the arbitration period. These methods only provide a strict priority access; the node with the highest arbitration number (closest to the root on a cable) will always win.

The Serial Bus adds a simple scheme that splits the access opportunities evenly among all competing nodes.

The fairness protocol is based on the concept of the "fairness interval". It consists of one or more periods of bus activity separated by subaction gaps and followed by a longer gap called an "arbitration reset gap".

At the end of each subaction gap, bus arbitration is initiated to determine the next node transmitting an asynchronous packet.

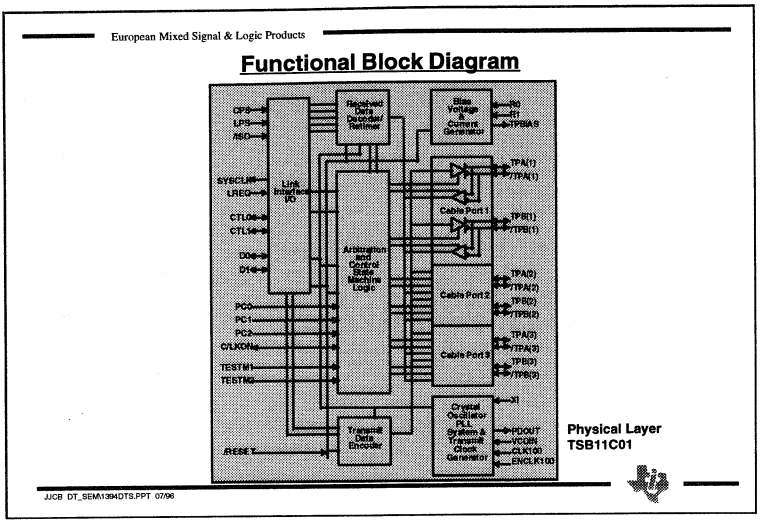


Fair arbitration allows for an active node to gain access to the bus ONCE during each fairness interval.

The process is described as follows:

1. An active node can only arbitrate if its arb_enable signal is set.
2. An ARB_RESET_GAP sets the signal to one and is cleared when the node wins arbitration and disables further arbitration requests from this node until the fairness interval ends.
3. The fairness interval ends when the final node has received successful arbitration.
4. An ARB_RESET_GAP is generated to re-enable arbitration on all nodes since the ARB_ENABLE signals are low and the nodes cannot drive the bus.
5. A new fairness interval starts.

NOTE: Natural priority of node A > node B > node C



Link Interface I/O

The TSB11C01 supports an optional isolation barrier between itself and its link-layer controller. When ISO' is tied high, the link-interface outputs behave normally; when tied low, an internal differentiating logic is enabled and the outputs become short pulses that can be coupled through a capacitor or transformer.

Received Data Decoder/Retimer

Decodes and resynchronizes the received data-strobe info. to the local clock to reduce system jitter accumulation.

Bias Voltage and Current Generator

Sets internal currents and cable driver output current. Also provides 1.86V nominal bias voltage needed to operate cables and to signal remote nodes that there is a valid cable connection.

Cable Ports

Transmitter/Receiver depending on flow of information. Data information on TPA diff. pair and strobe information on TPB diff. pair.

Crystal Oscillator PLL System and Transmit Clock Generator

Requires an external 25Mhz crystal or an external 100Mhz reference osc. The PLL provides 100Mhz for crystal input.

European Mixed Signal & Logic Products

Link Layer

- Provides the interface to the host
- Isochronous data transfer directly to the application
- Provides data transfer service between link and phy
- Transmits / Receives formatted 1394 packets

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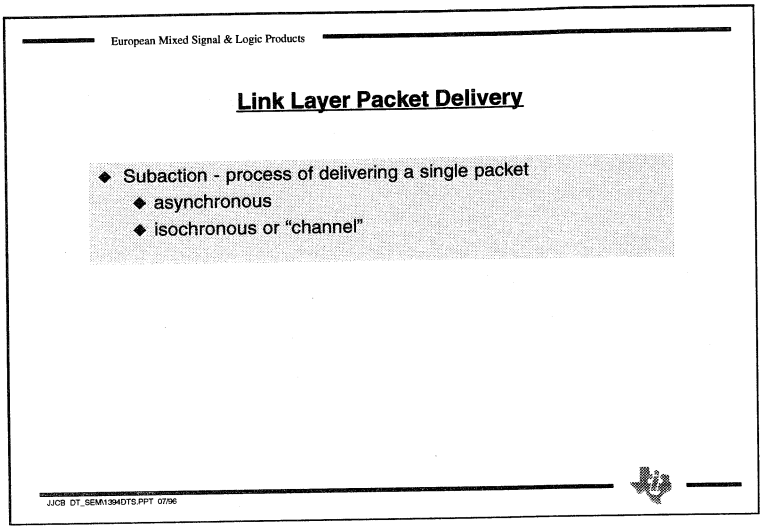
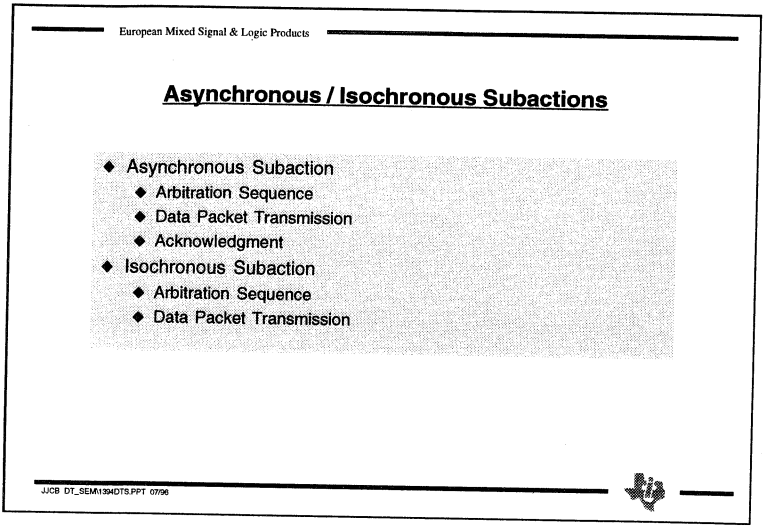


asynchronous - a variable amount of data and several bytes of Transaction Layer information are transferred to an explicit address and an acknowledge is returned

isochronous or "channel" - a variable amount of data is transferred on regular intervals with simplified addressing and NO acknowledge returned

Asynchronous Access Used when a Link Layer wants to send data as soon as possible.	VS.	Isochronous Access Used for data that needs a guaranteed bandwidth or a precise timing reference. Data such as digital sound or instrumentation is handled more conveniently.



Each subaction has three possible parts:

1. Arbitration Sequence - a node that wishes to transmit a packet requests the Phy Layer to gain control of the bus.

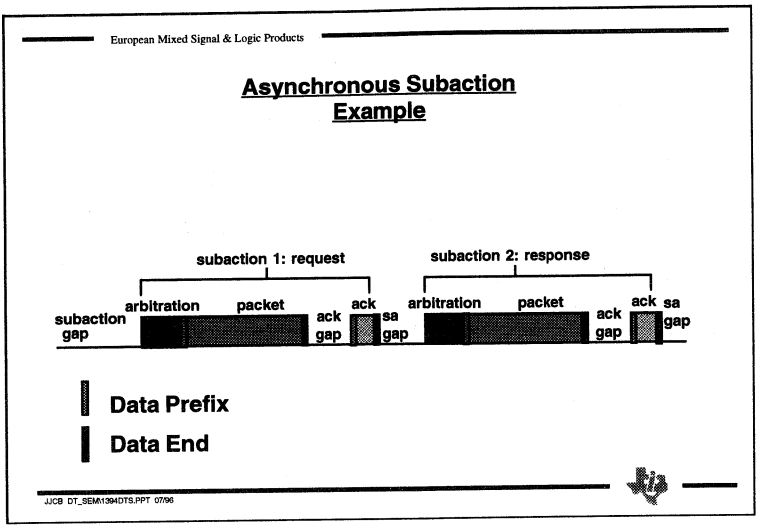
The Phy will respond immediately if the node already controls the bus (i.e. if the subaction is the transaction response corresponding to the immediately preceding acknowledge)

2. Data Packet Transmission - source sends a data prefix signal followed by: addresses of the source and destination nodes, a transaction code, a transaction label, a retry code, data, one or two CRCs, and a packet terminator.

NOTE: Isochronous packets have a short channel id instead of addresses

3. Acknowledgment - uniquely addressed destination returns code indicating action taken. Acknowledgment are also preceded by a data prefix and terminated by another data prefix or a data end.

NOTE: Isoch and Asynch broadcast packets have NO acknowledgment

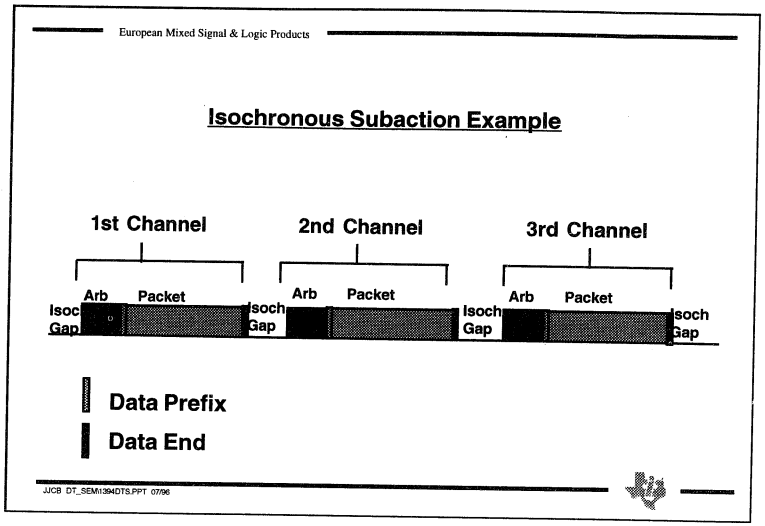


Subaction Gaps: periods of idle bus that separate all asynchronous subactions

Ack Gap: opens up on the bus between the packet transmission and the ack reception. It varies in length depending on location of receiver on bus.

NOTE: It will NEVER be longer than a subaction gap in order to ensure that other nodes will not begin arbitration before acknowledge is received.

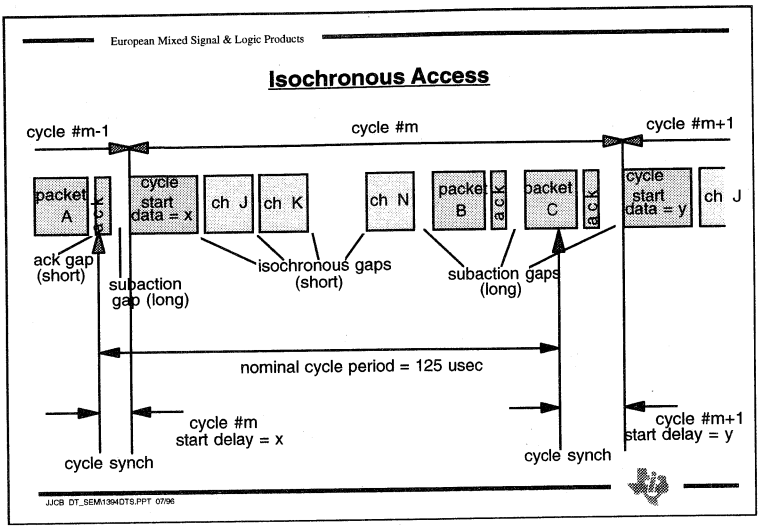
NOTE: Data prefix and Data end as specified in data packet transmission.



Every 125us there is a possibility for nodes to send isochronous data at the cycle synch pulse(explained later)

The % of bandwidth that may be consumed for isochronous data transfer in this period is 87.5%. Protocol allows isochronous data to transfer for 7/8 of the 125us period (i.e.=87.5%) while asynchronous data transfers on the bus for the remaining time.

The number of channels depends on the bandwidth of the data you are transmitting. There is no limitation as long as it fits within the specified time period.

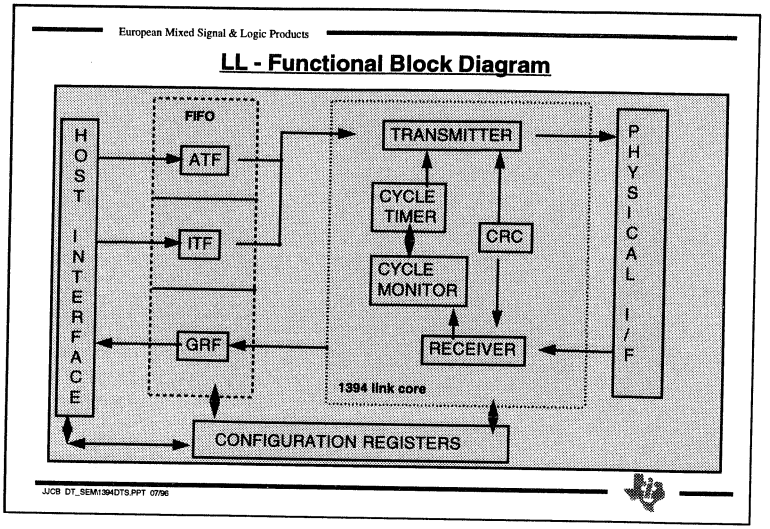


The "cycle master" or root node maintains a common clock source that tries to transmit a special timing request called a "cycle start".

A "cycle synch" pulse is sent every 125 us, and at this time if a "cycle start" request has been given by the isoch. master node AND no asynchronous data is on the bus, the isoch. data will pass on the bus.

If there is asynch. data on the bus at the cycle synch pulse when there is also a cycle start request by the root node, the asynch. packet will finish transmission and the iso. data will transmit at the end of the asynch. data packet.

The timing gaps between the isochronous data is smaller than those gaps needed for asynchronous arbitration to start. Therefore, after all the nodes have finished sending iso data they will stay quiet long enough for asynch arbitration to resume.



Physical Interface

Provides phy-level services to the transmitter and receiver. Including gaining access to the bus, sending and receiving data packets, and sending/receiving acknowledge packets.

Transmitter

Takes data from the Asynchronous-transmit FIFO or Isochronous-transmit FIFO (ATF or ITF) and creates formatted packets to be transmitted through the phy interface.

Receiver

Takes incoming data from the phy interface and determines if it is addressed to this node.

Transmit and Receive FIFOs

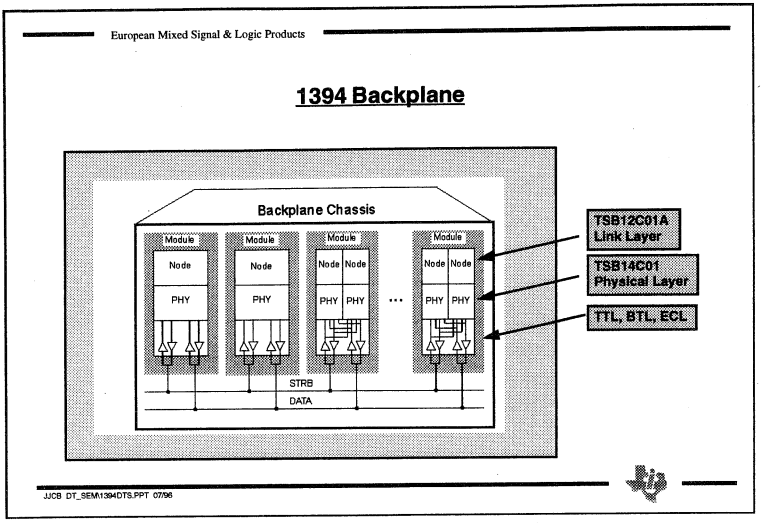
Two Transmit:

1. Asynchronous
2. Isochronous

One Receive:

1. General

NOTE: Length of these FIFOs is software adjustable! but must not exceed 508 quadlets



Backplane physical layer specification

The backplane environment physical layer provides the interface from a physical device to the backplane media. It provides arbitration services to permit a node to gain access to the bus, and performs the signal translations required to drive the bus and receive information from the bus.

Unlike the specification for the cable physical layer, the backplane physical layer specification does not include a description of connectors or media. Such documentation is assumed to be part of a host backplane specification or to be included in the requirements for the application environment.

The term "application environment" refers to the physical environment of the bus, the nodes, and the system that contains them. This environment may be a standardized host backplane (e.g., a FutureBus+ profile) that provides the signal requirements, a detailed description of the transceivers, the mechanical arrangement of the modules, and the temperature range over which operation is guaranteed.

The backplane physical layer shares some commonality with the cable physical layer. Common functions include: bus state determination, bus access protocols, encoding and decoding functions, and synchronization of received data to a local clock.

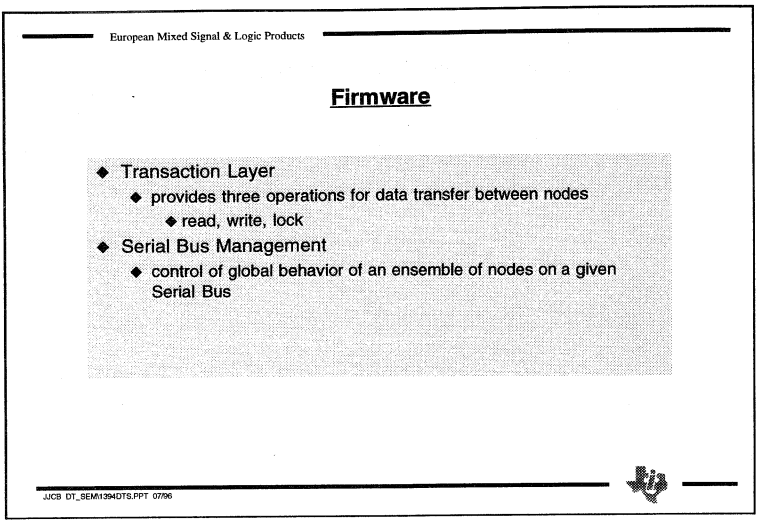
Backplane physical connection specification

Within the backplane environment the Serial Bus is implemented with a pair of signals: Strb and Data. The topology is a simple pair of bussed signals as shown.

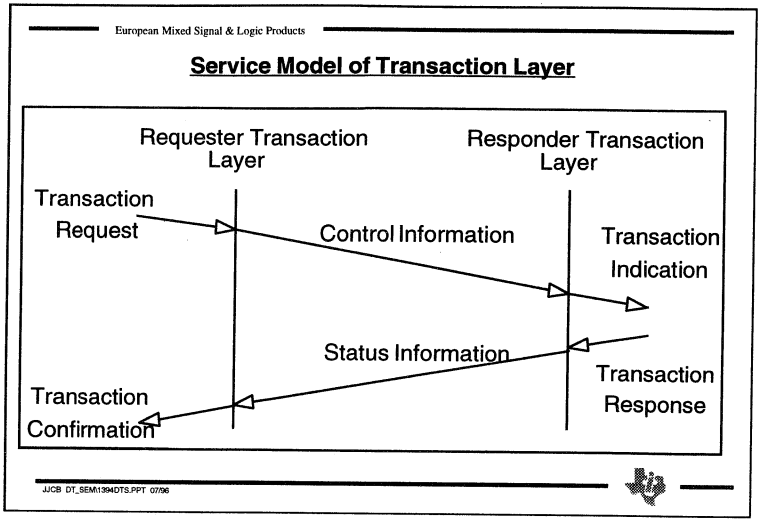
Backplane topology

The backplane environment can be implemented with a number of different interface technologies. These include, but are not limited to: TTL for industry-standard transistor-transistor logic, BTL for backplane transceiver logic as defined by IEEE Std 1194.1, and ECL for emitter-coupled logic.

In addition to the requirements specified by the application environment, the physical media of the Serial Bus shall meet the requirements defined for media attachment, media signal interface, and media signal timing. Timing requirements must be met over the ranges specified in the application environment. These include temperature ranges, voltage ranges, and manufacturing tolerances.



Transactions layer interacts between bus management, link layer and application.

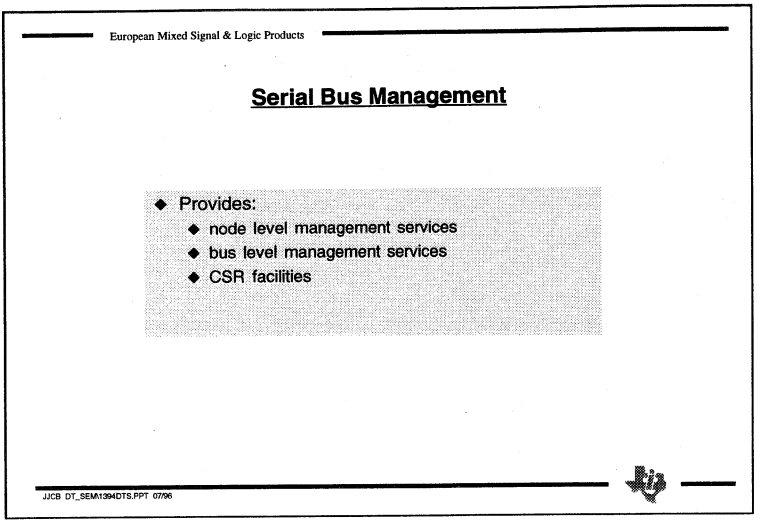


Data is transferred between nodes:

Data is sent to responder for write and lock operations

Data is sent back to requester for read and lock operations

If desired, multiple transactions may be in process at the same time. More than one transaction can be started by a requester before the corresponding response is returned.



These services are implemented in Software:

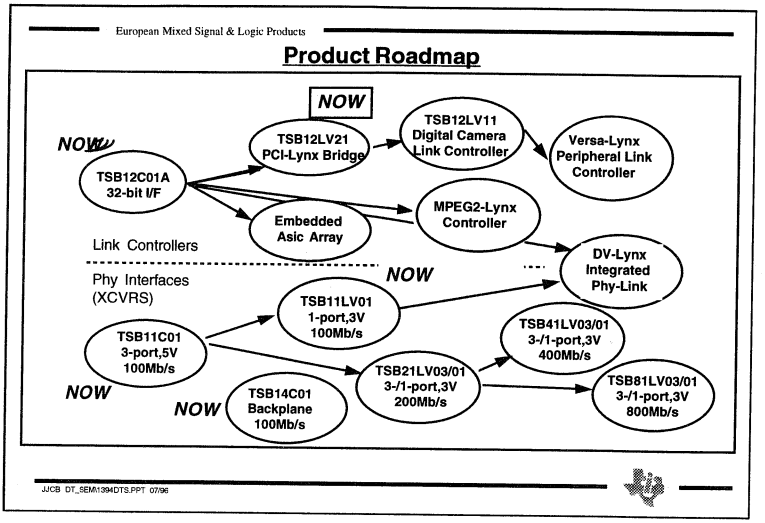
Node level management services:

control the operation of a given node and are discharged by the Node Controller component.

Bus level management services:

Control the relationship and interaction between nodes, and are discharged by the Full Bus Manager or the Limited Bus Manager components.

**Both of the above make use of the CSR (Control and Status Register) facilities



TSB12C01A Controller

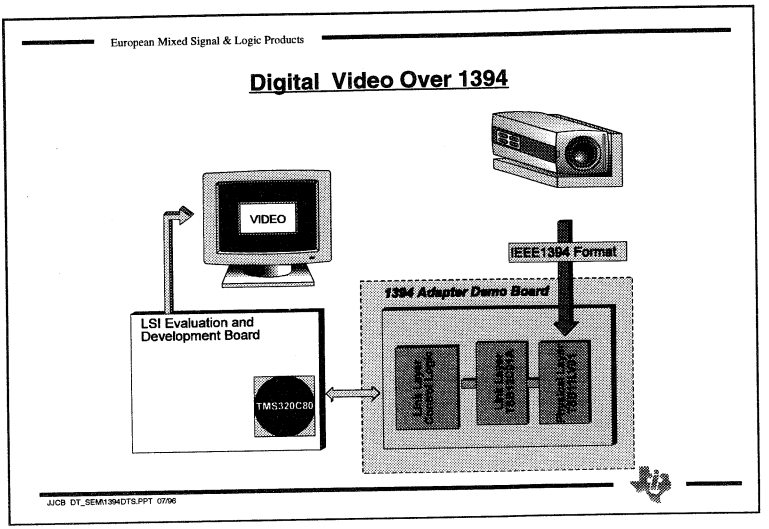
- Complies with IEEE1394 Serial-Bus Draft Standard
- Supports speeds of 100, 200 or 400 Mb/s
- Generic 32-bit host interface
- Contains Asynchronous-, Isochronous- ("Real-Time") Transmit, and General-Receive FIFOs
- Direct interface to TI's physical layer chips

◆PCILynx TSB12LV21

- Complies with PCI bus specification revision 2.0
- Supports Plug 'N Play specification
- Provides complete PCI-to-1394 solution
- Supports speeds of 100 and 200 Mbps
- Programmable FIFOs
- Five programmable DMA channels
- 8- or 16-bit zoom video (ZV) port for transferring data directly to an external video memory area; ZV port conforms to VESA and PCMCIA specifications
- Direct interface to TI's physical layer chips

- **Versa - Lynx TSB12LV31**
  - Complies with IEEE 1394 Standard
  - Programmable 8 or 16 bit microcontroller interface
  - 50 Quadlets (200byte) FIFO
  - Asynchronous receive/transmit via uC interface
  - Single DMA channel for isochronous transmits via ISO Write port
  - Isochronous receive buffered via uC interface or unbuffered via
  - ISO Write port
  - 3.3V supply operation with 5V tolerance
  - Packaged in 100-pin plastic thin quad flat pack (TQFP) package
- **TSB11C01 Physical Interface**
  - Interface directly to TSB12C01 Controller
  - Supports 100 Mbits/sec datarate
  - Contains three fully compliant IEEE1394 ports
  - Inactive ports are disabled to conserve power
  - System initialization and arbitration performance by on board-logic
  - Direct interface to TI's Link Layer chips
- **TSB21LV03 Physical Interface**
  - Complies with IEEE 1394 Serial-Bus Draft Standard
  - Supports speeds of 100 and 200Mb/s
  - Single 3.3V supply operation
  - Contains three fully compliant 1394 ports
  - Inactive ports are disabled to conserve power
  - System initialization and arbitration performance by on board-logic
  - Direct interface to TI's Link Layer chips

- **TSB11LV01 Physical Interface**
  - Complies with IEEE 1394 Serial-Bus Draft Standard
  - Supports speeds of 100 Mb/s
  - Single 3.3V supply operation
  - Contains fully compliant 1394 port
  - Inactive ports are disabled to conserve power
  - System initialization and arbitration performance by on board-logic
  - Direct interface to TI's Link Layer chips



Digital Video over 1394

The 1394 Adapter Demo Board interfaces to the IEEE1394 Serial High Speed Bus. The application is capable of being an isochronous listener and uses asynchronous transmission for performing CSR (control- & status register) functions.

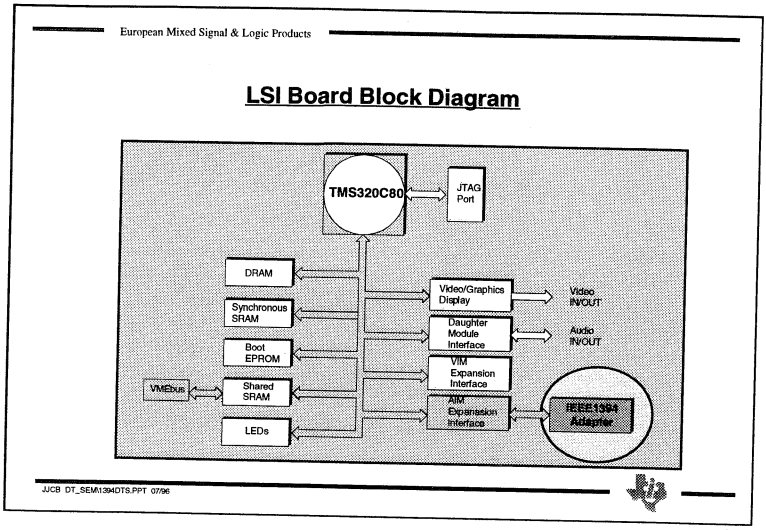
It also provides an interface to the Texas Instruments TMS320C80 Multi-Processor-DSP via the LSI (Loughborough Sound Images Ltd) TMS320C80 Evaluation and Development Board.

Link Layer Control Logic

- Interfaces to the lower 8 bits of the TMS320C80 address bus
- Uses to the upper 32bits of the 'C80 data bus
- Configures the external interface in the 'C80's transfer controller dynamically
- Converts 'C80 control signals to handle the required 1394 status and control function at the TSB12C01A host interface (Motorola 68XXX)

Transaction Layer

- Runs software on the C80 's Multi-Processor-DSP
- Asynchronous control of SONY digital desktop camera
- Transfers YUV data from GRF (General Receive FIFO) of TSB12C01A (Link Layer Controller) to frame buffer (located on LSI-Board), using packet transfers of the 'C80
- Converts YUV data to RGB
- Writes RGB frames to VRAM (located on LSI-Board)



LSI- TMS320C80 Evaluation and Developement Board

The TMS320C80 is accessible via the AIM (Application Interface Module) expansion interface, which provides almost all external C80 data address and control signals.

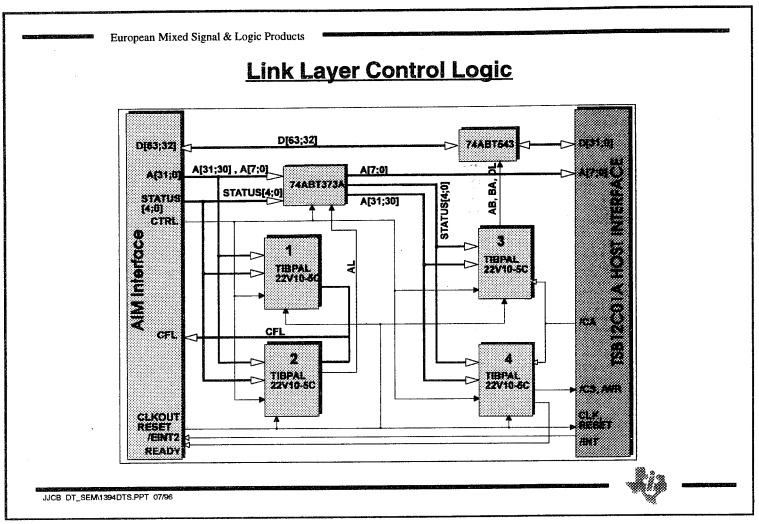
The IEEE1394 adapter board uses the Video/Graphics-Display and memory-units of the LSI board.

The 'C80 will take the transaction layer software for the 1394 node from the DRAM of the LSI board.

The memory-unit is used for frame buffering the YUV picture, coming from the 1394 adapter board. The 'C80 takes the buffered YUV data, converts them to the required digital RGB format and transfers them to the VRAM afterwards.

A Texas Instrument Video Palette transforms the converted digital RGB signals from the VRAM to analog RGB. The synchronization signals for the monitor are provided by the video controller of the 'C80.

An external monitor can directly be connected to the Video/Graphics Display unit of the LSI board using the analog RGB and synchronization signals.



Link Layer Control Logic

The Link Layer Control Logic provides the necessary functions for interfacing the TSB12C01A to the TMS320C80.

- PAL 1 and 2 are responsible for the configuration of the transfer controller in the TMS320C80

The status code (STATUS[0..4]), which is characeristic for the different read/write cycles of the 'C80 needs to be decoded and acknowledged by the control logic

After doublechecking the address and the status code the control logic generates the configuration data (CFL) required by the transfer controller of the 'C80

- The SN74ABT373 is to latch the status code coming from the 'C80 for further use by PAL3 and 4
- PALs 3 and 4 are responsible for generating the appropriate control signals to handle the read/write cycles for the TSB12C01A

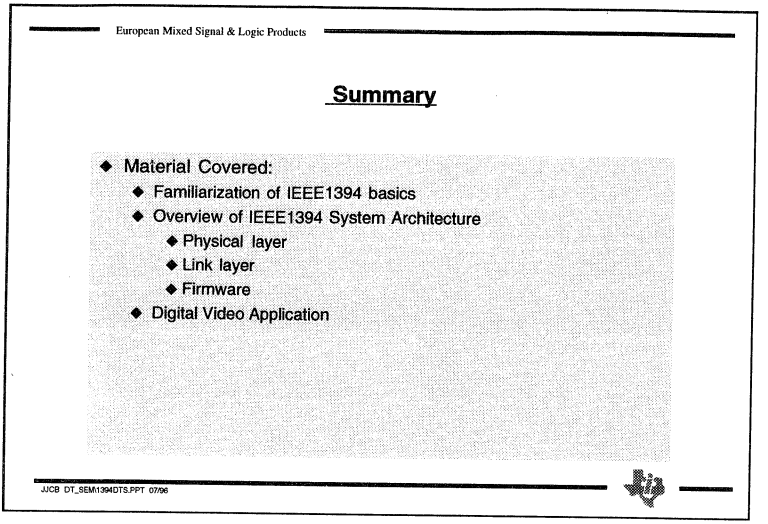
CS- Cycle Start

CA- Cycle Acknowledge

WR- Read/Write

- Additionally PAL3/4 generate the signals according to the data bus direction (D[0...31]) for the SN74ABT543.
- The SN74ABT543's function is to synchronize the outcoming data from the TSB12C01A to the 'C80. This buffering is necessary because of the synchronization barrier between the C80 cycles and the LinkLayer cycles.

Write cycles will not require such kind of buffering, because the data will still be active on the data bus during the whole cycle.



Recall for the physical layer:

1. Fairness protocol
   a. arbitration fairness for asynchronous data
2. Data-Strobe encoding
   a. ensures transition on either of the data or strobe lines one bit period apart for higher skew tolerance
3. Cable Configuration
   a. bus initialize
   b. tree identify
   c. self identify

Recall for the link layer:

1. Isochronous access
   a. every 125us isochronous data may be sent allowing for "same-time" transmission of data

Recall for system level architecture:

1. Transaction Layer
   a. provides three operations for data transfer: read, write, lock
2. Serial Bus Management
   a. control of global behavior of an ensemble of nodes

Where to Get More Information

- IEEE1394 IEEE Standard (800)678-IEEE
- Data Sheets:
  - TSB12C01A
  - TSB11C01
- 1394 Product Bulletin
- http://www.ti.com/sc/1394
  - Texas Instruments Web Pag
- http://www.firewire.org
  - 1394 Trade Association Wed Page

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